

Aspects of I/O filter design

Tim Williams
Elmac Services

e-mail timw@elmac.co.uk phone +44 1243 533361

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Contact:

Elmac Services, PO Box 111, Chichester, West Sussex, PO19 5ZS

Tel 01243 533361

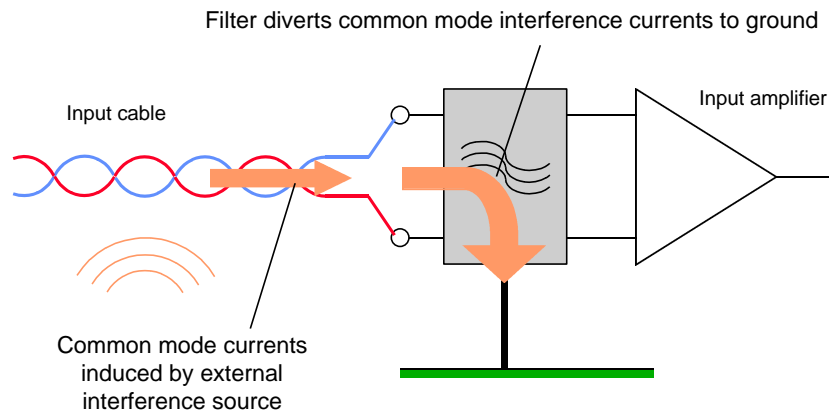
web: www.elmac.co.uk

- The purpose of an interface filter
- Typical circuits
- Model equivalent circuit for conducted immunity
- The problem of CM to DM conversion
- Some results and inferences

Interface filters are a common requirement in product design, especially for interfaces which do not enjoy the benefit of screened cables. This presentation discusses the basic need for a filter, particularly in the context of RF immunity performance, and goes on to look at a typical circuit that would be used to implement it. We see that an equivalent circuit model can be easily drawn up so that the RF performance of the filter can be determined by common software modelling packages.

In balanced signal interfaces, whether for analogue instrumentation or data, there is a particular issue which impacts on the performance required of a filter, and this is the degree to which a common mode injected signal is converted into a differential mode signal at the susceptible interface node. Some model results are shown which demonstrate that this conversion is particularly dependent on the capacitor components that are used in the filter.

The purpose of an interface filter

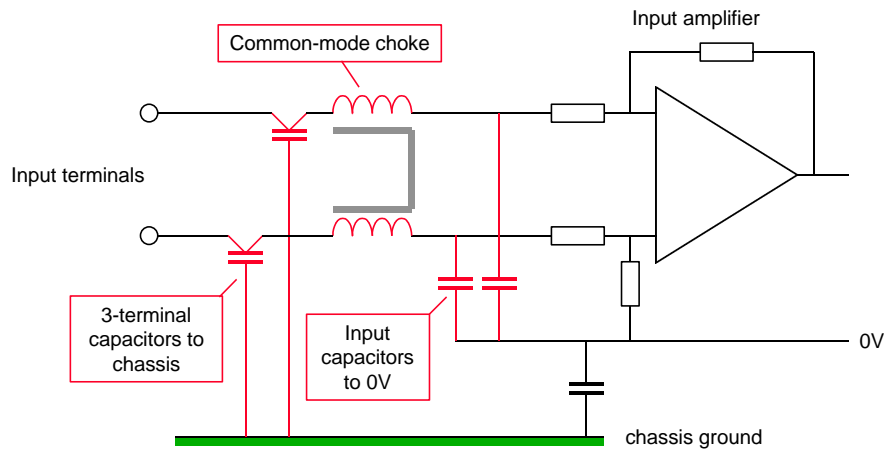


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The problem which affects all signal interfaces in respect of EMC is that external wires are subject to incoming disturbances which are induced in common mode on the cable. The sources of these disturbances can typically be radio transmitters, switching transients or lightning surges, and the immunity of the equipment is tested by the conducted and radiated RF, fast burst transient, and surge tests respectively. All of these phenomena are characterised by high frequency common mode coupling onto the cables and it is this mode that the filter is designed to combat.

It does this by providing a low impedance path to divert the disturbances to ground, and a high impedance path to block them from travelling into the operational circuit. The ground diversion of course relies on there being a suitable ground to carry the disturbance currents. This is fine if there is, for instance, a chassis or metal case which can provide this route; the EMC design must then ensure that this chassis creates a low-impedance path around or away from the circuit. If there is no such structure, then the disturbances have to be channeled to the circuit 0V, and the 0V layout must ensure that the disturbance currents don't affect the circuit. This is where a high-integrity ground plane is necessary.

Typical filter circuit

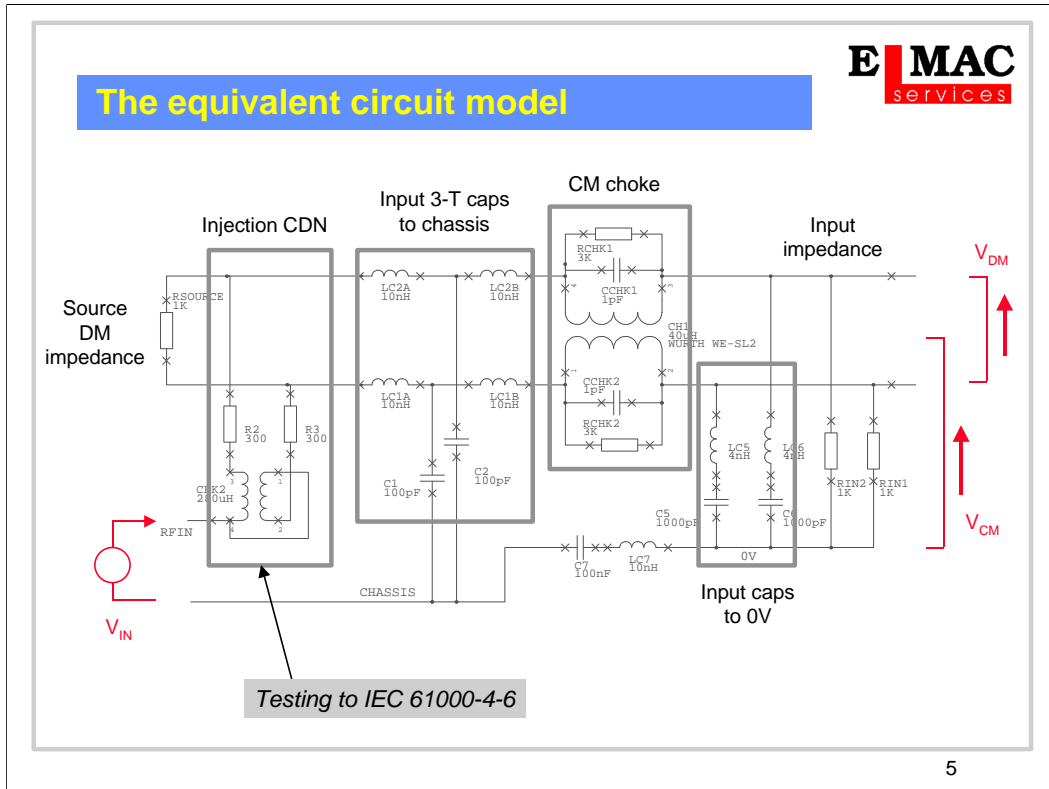


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The low impedance diversion to ground is provided by parallel capacitors, and the high impedance blocking is provided by a common mode choke (or by individual differential chokes) in series with the input. These components are shown in the example circuit above. Not necessarily all of these components will be present in a given design. The effectiveness of parallel capacitors or series chokes depends on the common mode source and input impedances in the circuit; a parallel capacitor is most effective into a high impedance while a series choke is most effective into a low impedance.

3-terminal capacitors are most effective in the high frequency range above, say, 50MHz where the self-inductance of ordinary chip capacitors limits their performance.

The full low-pass configuration shown here assumes that the disturbances have a higher spectrum than the wanted signals. For low frequency analogue instrumentation this is true, but it is not so by any means for wideband data or video signals. If such high-frequency wanted data is being transmitted, this will limit the value of the parallel capacitors and may rule them out altogether. It will not prevent the use of a common mode choke, since this is to a first order invisible to the wanted differential signals. For these applications the wanted signal is in the same frequency range as the interfering signal (150kHz – 80MHz for the conducted RF immunity test) and the only possible course is to prevent common mode interference from converting to differential.



The total equivalent circuit of the immunity test, including the injection mechanism, can be modelled to determine the effect of the filter components. This is shown in the circuit above, where individual segments are identified. Functional component values are largely arbitrary, and you should substitute whatever components you plan to use in your own application.

The cable is ignored for these purposes, although for completeness it should appear as a transmission line. The source impedance depends on the application, as does the input impedance of the circuit. In between, the injection coupling-decoupling network (CDN) is shown as two 300 ohm resistors (to give a 150 ohm source) separated by a differential mode blocking choke. The CDN could be modelled more completely with its high-frequency strays if desired. The input components – 3-t capacitors, C-M choke and input 0V capacitors – are modelled with their representative stray reactances, which can be derived from the manufacturer's data and a knowledge of the circuit layout. These should be included for a proper understanding of the high frequency performance.

The model is set up to provide the transfer function between V_{IN} , the applied voltage at the injection point (3V or 10V in the IEC 61000-4-6 test) and either V_{DM} or V_{CM} , the differential and common mode voltages at the operational circuit input.

Conversion from CM to DM

- If all the components (R, C and L) in the two halves of the differential circuit are exactly balanced, there is no CM-to-DM conversion:

$$|V_{DM}|/|V_{CM}| = 0$$

- but if there is any imbalance in any component in the two halves of the circuit, some differential mode voltage results:

$$|V_{DM}|/|V_{CM}| > 0$$

- the most likely source of imbalance is in the capacitor values, which can easily be $\pm 20\%$

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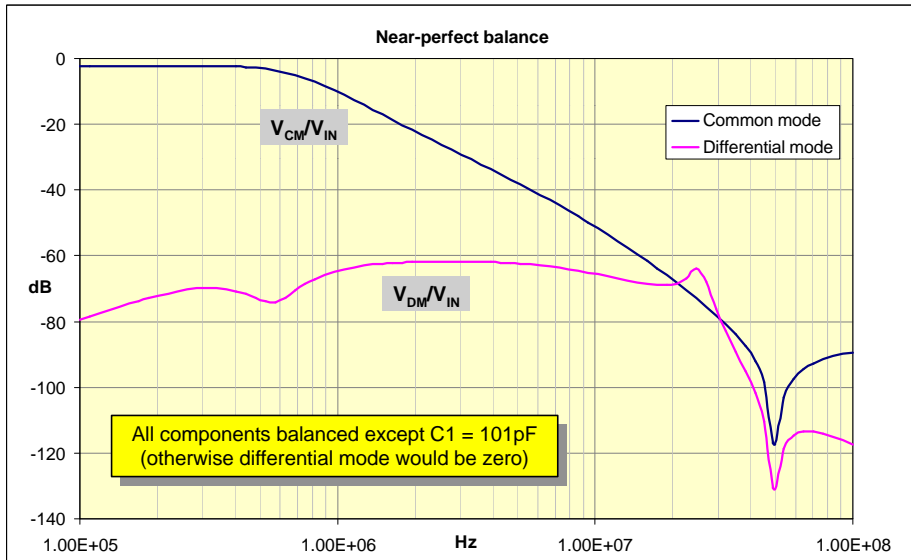
The significant issue for balanced circuits is the degree to which the filter components influence the common-to-differential mode conversion. The common mode RF attenuation is increasingly effective as the frequency rises, as expected. But at the lower frequencies, there may be some conversion of the common mode disturbance into a differential mode input, which of course cannot be rejected by the input amplifier.

If the entire circuit is balanced, then this conversion does not occur. But actually maintaining balance requires that every component in one half of the circuit exactly mirrors that in the other: not only its primary value but also the value of its stray reactance. This is not easy to achieve. In the common mode choke, the construction of the windings will cause a small degree of imbalance in the inductance of each half and in the stray capacitance associated with each half. But if discrete components are used for the capacitors, these are usually the dominant source of imbalance: tolerances on these capacitors depend on their construction, but COG ceramic capacitors are typically $\pm 5\%$ or $\pm 10\%$, while X7R can easily be $\pm 20\%$. Some capacitor types, intended specifically as I/O filters, have tolerances as wide as $+50\%$ -20% .

- The following graphs show model results for the previous equivalent circuit:
 - transfer function versus frequency, 100kHz – 100MHz
 - for differential mode (V_{DM}/V_{IN})
 - and common mode (V_{CM}/V_{IN}) (first slide only)
- for different conditions of balance and unbalance in various components in the equivalent circuit

Taking this issue into account, the model circuit shown earlier was run to give a transfer function versus frequency, over the range of interest for the conducted RF immunity test, for the filter circuit in both differential and common mode. The component values were varied to give different conditions of balance and unbalance. Just a few results are shown here: it is recommended that you do this yourself for your own circuits, and vary the components appropriately to get an idea of how your particular filter might perform.

Model results: initial assumptions



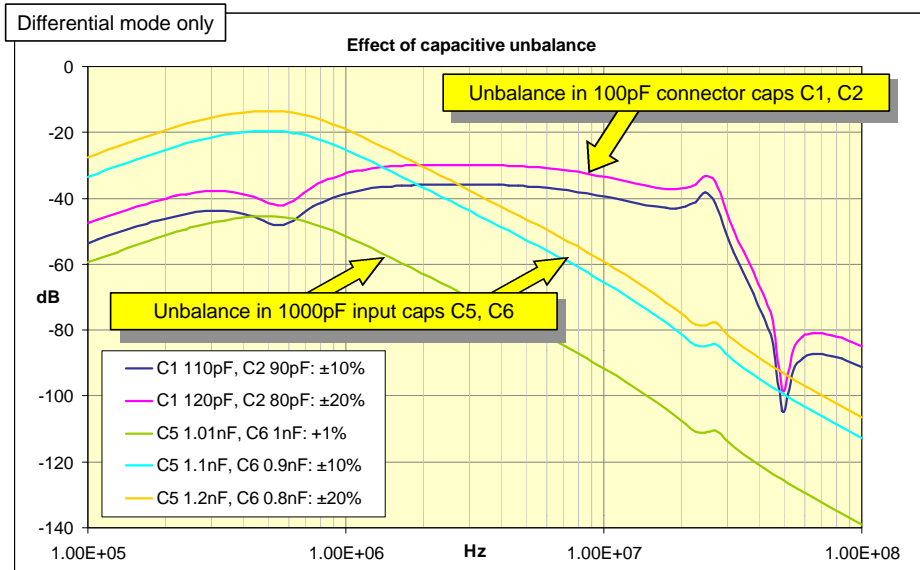
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The first graph, above, shows the common mode attenuation (dark blue) for the standard, fully balanced circuit. This shows negligible attenuation at the bottom end, increasing to better than 50dB above 10MHz. Component values could of course be increased to improve the low frequency attenuation, although for many circuits the LF common mode rejection of the input amplifier is adequate on its own. The scaling is easy to interpret: an attenuation of 20dB, for instance, means that if the injected voltage is 10V then a 1V disturbance appears at the input terminals, either in common or differential mode.

The magenta curve shows the differential mode rejection. If the components were all exactly balanced then no conversion would occur and the trace would be off the bottom of the graph, so one of the input 3-t capacitors (C1) has been increased in value by 1% to 101pF. This is sufficient to bring the differential mode attenuation up to around -60dB over much of the mid frequency range: an input of 10V would create 10mV of disturbance, not enough to upset data communications, and probably not enough to worry a well designed instrumentation amplifier either.

Unfortunately, the idea that just a single component might be unbalanced by only 1%, and all others exhibit perfect balance, is pretty much pie in the sky.

Model results: capacitive unbalance

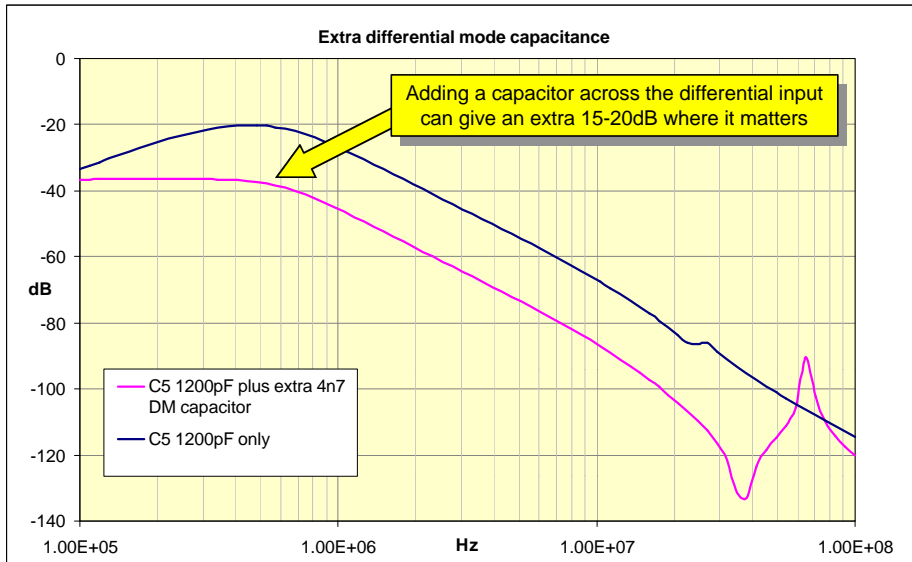


When worst-case tolerances are put into the model, a different picture emerges. If the 100pF capacitors only are unbalanced, then as might be expected, the effect is limited by the perfect balance in the 1000pF capacitors; but even so, a 20% excursion in the 100pF parts worsens the conversion to -30dB (the magenta curve). And this effect is maintained out to 25MHz.

If instead the 1000pF input capacitors are unbalanced, a significant extra feature emerges: the common-to-differential mode conversion is much worse, at the lower frequencies. For a 20% excursion in these values, the conversion is a mere -14dB around 500kHz. A 10V injected signal would give 2V of differential disturbance, very likely in-band for a typical digital datacomms application, and probably leading to a susceptibility.

Of course, the worst case is an imbalance in the same direction in each of the capacitor value pairs, perhaps augmented by imbalance in the common mode choke. That isn't shown here, but you can try this on your own circuit. This points up another consequence of component imbalance: if your test results are gained on a sample where the balance is good, perhaps within 1%, you may find completely different (and substantially worse!) results when you test a different but notionally identical sample, with worst case component imbalance. Add this to the known problems of repeatability of these immunity tests, and you can see that the likelihood of getting a predictable immunity performance between different units and different test facilities is slim indeed.

Model results: mitigation



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How can the CM-to-DM performance of an input filter be improved? There are several options:

- reduce the value of, or even eliminate, the capacitors. This will reduce the conversion but will also reduce the common mode attenuation, although it may still be adequate at the higher frequencies, and means that the filtering is almost entirely reliant on the CM choke.
- Add a capacitor across the differential mode input, i.e. the tops of C5 and C6 (see graph above). This has no effect on the CM attenuation but the model shows that it is effective in reducing the DM conversion in the worst area of the frequency range. Naturally, it reduces the wanted signal bandwidth.
- Ensure better balance in the filter capacitors. We've been assuming an imbalance of at least 5%, possibly up to 20%. However, capacitor arrays can usually achieve a balance between the individual components on the array of 1%, although the manufacturers don't guarantee it; and they also use less overall space on the board. Although the value tolerance is no better than individual parts, this is far less important than the variations between parts in the balanced circuit. Alternatively, X2Y components are now readily available and also offer a good match between the two Y-components, as well as a construction which allows good grounding, so these can be considered.

Conclusions

- Modelling shows that you have to be careful about imbalance in differential interface circuits, especially related to capacitor value tolerances
- Common mode attenuation is easily achievable but common to differential mode conversion may be significant
- Modelling the circuit to adjust the values is easy:

YOU CAN DO THIS AT HOME, KIDS!

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In summary, the filter requirements for balanced interfaces encompass not only good common mode attenuation but also good rejection of CM-to-DM conversion. This means that capacitor tolerances, in particular, need to be carefully evaluated. A straightforward means of doing this exists in a CAD model of the interface equivalent circuit, which takes into account the injection mechanism as well as all the relevant stray parameters around the actual components.

Designers are recommended to use such a model with vigour in the early stages of their design process. It will add a quantitative, predictive dimension to the sadly too-frequent approach of “we did it this way last time and it worked” or “these are the components we’ve got in stores”.