Daniel Winkelstein

2308 Lawrence Dr. Raleigh, NC 27603-2627
(919) 418-1507 (C) (919) 832-5542 (H)
e-mail: dan.winkelstein@ieca-inc.com

Electrical Engineering Design and System Architecture Technology Consultant

OVERVIEW AREAS OF EXPERTESE

- Encryption: DES, 3DES, AES, RSA, MD5, SHA-1, others
- High Speed Digital Design: XAUI, PCIe, Interlaken, 10GBase-KR
- Network Processor Design: Marvell AX240, EzChip NPA, Intel IXP2400
- Memory Design: DDR2/DDR3 SDRAM, QDR SRAM, NAND, NOR
- Processor Design: PowerPC, Cavium MIP, Intel IXP425 (ARM v7)
- Communications: Ethernet: 10GBase-X, 10/100/1000Base-T, SONET, ATM, RS-232, PPP, MLPPP, X86, DS-3, DS-1
- Signal Integrity Analysis: Hyperlynx, HSPICE, Cadence Allegro PCI SI
- CAD tools: Mentor Graphics DxDesigner, Cadence Allegro, OrCAD, PADS
- Operating Systems: Linux, VxWorks
- FPGA/CPLD Design: Altera, Xilinx, Lattice designs in VHDL and Verilog
- Software: C/C++ for Linux device drivers and Hardware Abstraction Layer
- Testing: EMI, ESD, Homologation, HALT/HASS, JTAG, BIST
- Timing: IEEE 1588v2, Sync-E, SONET

PATENTS

US Patent US 2003/0196081A1, October 16, 2003
"Methods, Systems, and Computer Program Products for Processing a Packet-Object Using Multiple Pipelined Processing Modules"

US Patent US 2001/0042204A1, November 15, 2001
"Hash-Ordered Databases and Methods, Systems and Computer Program Products for use of a Hash-Ordered Database"

US Patent: 5,025,402, June 18, 1991
"Method of Transient Simulation of Transmission Line Networks using a Circuit Simulator"

PROFESSIONAL EXPERIENCE

Overture Networks	**637 Davis Dr. Morrisville, NC 27560**	**October 2008 - October 2012**

Senior Staff Engineer
Chief architect and principal hardware designer for Carrier Ethernet class aggregation and customer premises products.

Multi-10Gbps Carrier Ethernet Class Aggregation Product Family
Chief architect and hardware designer: I was personally responsible for the hardware and system design for a 7-card chassis based product that supported 8 10GBase-X and 72 1000Base-X Ethernet interfaces. I designed the NPU based distributed dataplane processing complex (using multiple Marvell AX240) that performed high touch Layer-2 and Layer-3 packet processing with a combined bandwidth of 334MPPS. I designed the 20Gbps dataplane interconnect used for card-to-card communication. Additionally, I

designed the system wide distributed control plane processing based on the multicore Cavium family of MIPs processors.

1 Gigabit Carrier Ethernet CPE Product Family for Ethernet transport over TDM Networks
Chief architect and hardware designer: I was personally responsible for the control plane and dataplane main board design. This product used a Cavium MIPs processor and an Altera FPGA for dataplane and control plane processing. This product had a highly aggressive schedule: start-to-customer GA in only 9 months for a brand new design.

SafeNet (Formerly Cylink and Celotek)	**951 Aviation Parkway Suite 300 Morrisville, NC 27560**	**October 1996 - October 2008**

Principal Scientist
Security Clearance: Top Secret
Founding partner in a startup corporation. Principal hardware and system architect for a set of encryption products for ATM, SONET, Ethernet and IPSEC networks.

10 Gigabit Ethernet MACsec Product Line: Chief architect, hardware designer, and FPGA designer for a MACsec, standard based, high performance Ethernet security encryption solution: I designed a high performance 10Gbps Ethernet solution based on XFP transceivers, Marvel 10G PHY devices, Cortina 10G MAC devices and Stratix-II FPGAs. Personally responsible for the hardware design of the Ethernet encrytion devices including the security and host processor complex. This design uses Safenet developed Intellectual Property for MACsec encryption and KEYsec key exchange. I was personally responsible for ensuring that the Intellectual Property developed, at four geographically remote locations, integrated smoothly in addition to designing the hardware and architecting the system.

OC-192 Type-1 SONET Encryption Product Line: Team member and system architect of a 10Gbps Classified SONET encryption product line: I was personally responsible for the hardware design of the 10Gbps SONET interface card and a 2.5Gbps SONET interface card. The design included advanced PLLs for clock management, Agere ASICs, and Altera Stratix-II FPGAs. Additionally, I was responsible for the Verilog HDL design for four large FPGAs.

Gigabit IPSEC Gateway Product: Chief hardware architect and designer for a multi-Gigabit IPSEC encryption product based on a dual IXP2400 Network Processor and VxWorks operating system: I designed an embedded Network Processor based dataplane processing system with interfaces to QDR SSRAM, DDR SDRAM and Xilinx Virtex-II FPGAs.

Cost reduction team leader: Chief architect and hardware designer for a cost reduction effort that reduced the CoGs of our encryption products by more than 75%.

ASIC design: Team member of a three-man design team that produced a 250,000 gate ASIC for an OC-3c rate ATM encryption product.

ATM encryption product: **A**rchitect for an FPGA based ATM encryptor that operated at rates from 1.5Mbps up to 622Mbps full duplex: As part of a startup, I was personally responsible for hardware design, FPGA design, PCB board design, as well as some software design.

MCNC	**3021 Cornwallis Rd, Research Triangle Park, NC 27709**	**July 1990 - October 1996**

Communications Research Engineer
Security Clearance: Top Secret
Principle Investigator and hardware designer for state-of-the-art research projects in communication, data encryption and network security.

ATM traffic analysis and encryption research: Principle investigator of a series of DARPA funded projects to design, build, and test the traffic characteristics and security of OC-12c rate ATM networks: I designed the hardware for the first demonstrable non-classified encryption technology for ATM networks operating at OC-12c rates.

ATM networking research: Hardware designer for a DARPA/NFS funded project to prove the feasibility of distributed supercomputing over high speed wide-area networks: I was responsible for the hardware design for an 800Mbps traffic analysis system.

Nortel (Formerly BNR Inc.)	**35 Davis Dr. Research Triangle Park, NC 27709**	**July 1985 - July 1990**

PCB design research: I was team leader of a research group that investigated transmission-line effects of printed circuit board design on high-speed digital signals.

Central Office switching equipment design: I was part of a group that designed Telco-class central office switching equipment. I was responsible for the design of the power subsystems and cable assemblies.

EDUCATION

North Carolina State University	**Raleigh, NC**	**September 1986- June 1989**

Masters of Science in Electrical Engineering
Advisor: Michael Steer
Master's thesis: "Transient Simulation of Arbitrary Transmission Line Networks with for Non-Linear Termination"
For this research project, I developed a method to simulate transmission line effects in a lossy environment with non-linear termination. This simulation included both single line and cross-talk associated with multi-line transmission lines on printed circuit boards.
Publication: D. Winkelstein, M. B. Steer and R. Pomerleau, " *IEEE Trans. on Circuits and Systems,* April 1991, pp.418-422. See also, *IEEE Trans. on Circuits and Systems,* Vol. 38, Oct. 1991.

Rensselaer Polytechnic Institute	**Troy, NY**	**September 1981- May 1985**

Bachelor of Science in Computer and Systems Engineering