



Practical Papers, Articles and Application Notes

Robert G. Olsen, Technical Editor

In this issue you will find three practical papers that should be of interest to members of the EMC community. The first is entitled “PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?” by James L. Knighten, Bruce Archambeault, Jun Fan, Giuseppe Selli, Liang Xue, Samuel Connor, and James L. Drewniak. This is the second in a series of papers they are writing. If you enjoyed the first paper published in the Fall 2005 issue (and I suspect that you did), you will enjoy this one. As I noted last time, the speed of digital systems is increasing and the subject of power supply decoupling is more relevant than ever. The second paper is entitled, “Electromagnetic Near-Field Scanning for Microelectronic Test Chip Investigation” by Adam Tankielun, Uwe Keller, Etienne Sicard, Peter Kralicek and Bertrand Vrignon. In this paper the authors discuss the effects of on-chip decoupling capacitors in the power supply network of a CMOS test-chip on radiated noise. It is a nice complement to the first paper in this section. The third paper is entitled, “Selected Methods for Validating Computational Electromagnetic Modeling Techniques,” by Andy Drozd. In Andy’s words, “Computational electromagnetics and computer technique validation is a very hot topic at the moment, not just within the EMC Society circles, but elsewhere and with-

in other EM consortia.” I agree and believe strongly that the use of numerical techniques without a concern for their validity can lead to serious problems. This paper was first presented at the 2005 IEEE International Symposium on EMC in Chicago and has been reprinted here by permission of the Symposium Committee.

The purpose of this section is to disseminate practical information to the EMC community. In some cases the material is entirely original. In others, the material is not new but has been made either more understandable or accessible to the community. In others, the material has been previously presented at a conference but has been deemed especially worthy of wider dissemination. Readers wishing to share such information with colleagues in the EMC community are encouraged to submit papers or application notes for this section of the Newsletter. See page 3 for my e-mail, FAX and real mail address. While all material will be reviewed prior to acceptance, the criteria are different from those of Transactions papers. Specifically, while it is not necessary that the paper be archival, it is necessary that the paper be useful and of interest to readers of the Newsletter.

Comments from readers concerning these papers are welcome, either as a letter (or e-mail) to the Technical Editor or directly to the authors.

PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?

James L. Knighten¹, Bruce Archambeault², Jun Fan¹, Giuseppe Selli³, Liang Xue³, Samuel Connor², and James L. Drewniak³

I. INTRODUCTION

This is the second in a series of papers on design strategies for effectively decoupling dc power distribution networks (PDN) on digital printed circuit boards (PCB). The first paper examined means for choosing the values of high-frequency decoupling capacitors when designing multi-layered PCBs intended for digital circuits with medium-to-high-speed switching speeds [1]. Methods that are frequently in use in circuit design communities, i.e., the signal integrity community and the EMI/EMC design community were compared. One of these communities is inclined to work in the time domain and the other is more inclined to work in the frequency domain. While engineers of both communities wrestle with the same physics of the dc PDN on a digital PCB, they may perceive the same physical phenomena differently. In the end, however, engineers

from both communities have similar goals of assuring adequate charge transfer between active devices on a PCB and designing a PDN with minimum noise generation.

Decoupling capacitors on a PCB are important design factors in mitigating noise in the power bus or the PDN. Noise is generated in the power bus when a digital active device switches between its high and low logical states (switching noise), or it can be coupled to the power bus when a high-speed signal transits through the power bus by signal vias (transition noise). A good PCB design ensures that the generated noise be constrained to a level that permits successful circuit operation and the resulting low levels of radiation produced do not violate regulatory requirements.

This paper examines the question of whether specific locations of high-frequency decoupling capacitors on a PDN can be

¹NCR Corporation, San Diego, CA, jim.knighten@ncr.com and jun.fan@ncr.com

²IBM Co., Research Triangle Park, NC, barch@us.ibm.com and sconnor@us.ibm.com

³University of Missouri-Rolla, Rolla, MO, gs5xd@umr.edu, lx239@umr.edu and drewniak@umr.edu

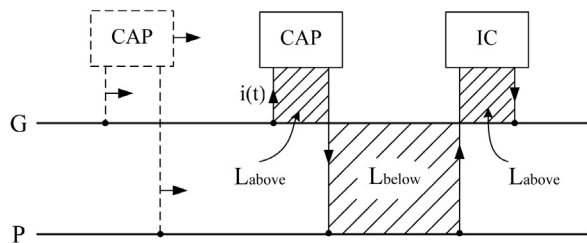


Figure 1: The inductance in the current path between IC and decoupling capacitor includes inductance elements above and below the planes, as shown by the regions of magnetic flux enclosed by the current path.

significant, or, if all decoupling capacitors behave such that it does not matter where they are placed. This paper shows that most decoupling capacitors behave globally, but there are cases where capacitor location matters. Additionally, this paper examines the conditions required for location to be significant. This paper examines the significance of capacitor location using both the frequency and time domain analyses.

The inductance associated with a decoupling capacitor (including its connection inductance and its ESL) greatly affects the effectiveness of the capacitor over a broad frequency range [1]. The inductance (often parasitic) in the capacitor's circuit is what determines the capacitor's ability to either absorb or release charge rapidly. The lower the value of this series inductance, the faster the capacitor can move charge and the more importance that may be attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior, depending on the relationship of the inductances above and below the plane as will be shown.

The significance of decoupling capacitor location has been extensively studied in the EMI design community [2, 3]. In the early days of digital electronics on PCBs consisting of only a few layers (and perhaps without power and ground planes), the conventional wisdom was that decoupling capacitors should be placed as close as possible to the major active components. Within the past decade, the conventional wisdom for digital electronics on multilayered PCBs with planes (which is the model for modern high-speed digital design) has been that it is not generally necessary to relate the effectiveness of the decoupling capacitors to their distance with respect to the IC's, i.e., the decoupling capacitors behave in a global manner [4]. More recent work indicates that there are specific situations where the proximity of the decoupling capacitor to the IC can have a strong influence of the effectiveness of the capacitor [5]. Hence, there is a growing acceptance that there are specific design situations where it is beneficial for the capacitor to be placed "close" to an IC power pin.

Figure 1 shows a conceptual configuration of an IC and a decoupling capacitor attached to a power bus. The current loop formed by the IC drawing current from the power bus and capacitor has three distinct regions of magnetic flux that define the inductance of this loop. The regions labeled L_{above} represent the inductance of the connection between IC and plane and between capacitor and plane. (The two L_{above} regions are not necessarily identical, but they are treated as such in this discussion.) The region labeled L_{below} represents the inductance of the portion of the current loop that exists between the power and ground

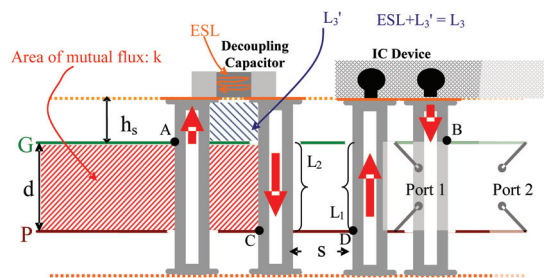


Figure 2: The physics of the local decoupling behavior are viewed by looking at one decoupling capacitor and only one PWR/GND pin pair from an IC device. The area of mutual flux, the coupling coefficient k , and the ratio L_3/L_2 quantify the effect of local decoupling.

planes. L_{below} has a self inductance component and a mutual inductance component which represents mutual coupling (transformer-like) between the two vias. The mutual inductance acts in opposition to the self-inductance and reduces the overall value of L_{below} . The total loop inductance encountered by the current flow from IC to capacitor is the sum of these inductances,

$$L_{Total} = 2L_{above} + L_{below} \quad (1)$$

If the capacitor were moved closer to the IC, as indicated by the dashed lines in Figure 1, then the vias that form the boundaries of L_{below} become closer, the increased mutual magnetic coupling between these vias decreases L_{below} causing L_{total} to decrease. (The decrease in L_{below} due to mutual coupling is explained later in the discussion of Figure 2.) Recall the earlier assertion that the lower the inductance value, the faster the capacitor can supply and store charge and the more importance may be attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior. Therefore, this decrease in inductance should enhance the effectiveness of the decoupling capacitor and may render decoupling effectiveness that is more apt to be location-dependant.

Why then isn't high-frequency decoupling capacitor location always an important factor in effective decoupling? The reason is that the overall inductance is not always substantially reduced by moving the capacitor closer to the IC. This is the case when the L_{above} inductances are considerably larger than L_{below} . Much of the following discussion addresses the question of how close is close enough. The answer is not easily answered in specific terms because effective location-dependent decoupling depends on several parameters.

II. MAGNETIC COUPLING BETWEEN VIAS CAN AFFECT DECOUPLING

The function of a decoupling capacitor is to provide charge for active device logic state transitions and to reduce the propagation of power bus noise [1]. Therefore, the effectiveness of a decoupling capacitor may be measured by its effectiveness in supplying charge (but more often measured by the power bus voltage perturbations during transition, i.e., voltage ripple) with suitable promptness and its ability to reduce the PDN impedance, although these measures may not be independent.

A decoupling capacitor that behaves globally supplies charge

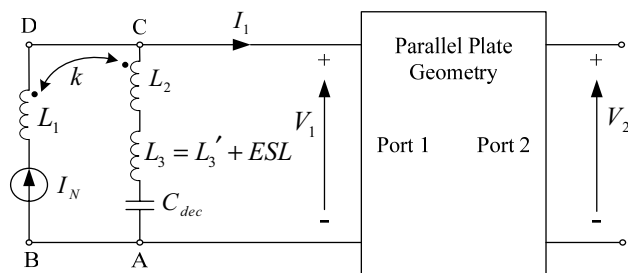


Figure 3: The equivalent circuit of Figure 2 showing the mutual coupling between capacitor and IC vias and the connection to Port 2 of the power bus.

to the entire ensemble of ICs connected to a PCB PDN so that its location is not important to its effectiveness. For a capacitor that behaves globally, the primary parameter of interest is the frequency range over which the decoupling capacitor is able to lower the impedance of the PDN. This frequency range is limited by the series resonant frequency of the decoupling capacitor and its interconnect. At frequencies higher than this limit, the capacitor behaves inductively, rather than as a capacitor, and does not perform the decoupling function of lowering the power bus impedance.

On the other hand, the location of a decoupling capacitor may be important in meeting the special needs for charge delivery for a particular IC, as well as reducing the power bus noise generation by this IC. In such a case, the location of the decoupling capacitor is important and the capacitor is described as exhibiting local decoupling behavior. It is important to note that there is no physical difference between a decoupling capacitor that is used in a global manner or one that is used in a local manner. The differences are in the environment in which the capacitor is placed [2, 3, 5].

During initial switching of states in an IC, current is drawn from the planes of the power bus, followed by current drawn from decoupling capacitors [1]. Two important indicators in assessing if a capacitor behaves in a local manner are: (a) the current available to the IC is significantly dependent on the location of the capacitor, and, (b) the voltage of power bus is significantly affected by the location of the capacitor. Intuitively, the closer a decoupling capacitor is located to an IC's power pin, the more rapidly charge is able to traverse the distance between the two components. Also, intuitively, the greater the inductance in the current path from the capacitor to the IC's power or ground pin, the less rapidly charge is available to the IC and the less important the proximity between the two. (Subsequent discussions show that location dependence of the capacitor can relate to proximity of either the IC power or ground pins.)

The ability for rapid behavior is directly related to the inductance of the capacitor's interconnect and its ESL. However, two identical capacitors with identical interconnect may still differ in their abilities to exhibit local decoupling behavior. The reason for this is the degree of magnetic coupling that exists between the vias of the power/ground connections of the IC and the decoupling capacitor, as shown in Figure 2. The mutual coupling between the vias reduces the overall interconnect inductance that determines the magnitude and rapidity of the charge supplied by the capacitor. (The reduction of overall inductance can be seen in

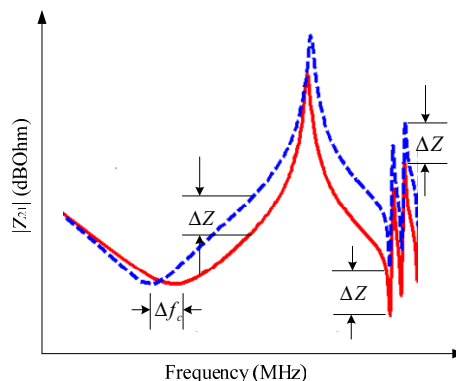


Figure 4: The mutual coupling between IC and capacitor vias that are in close proximity (a) increases the series resonance of the capacitor and (b) lowers the power bus impedance uniformly (approximately) for frequencies above the series resonance. The red solid trace indicates increased mutual coupling between vias than is the case for the blue dashed trace.

Figure 2, where the directions of the currents in the two vias produce magnetic flux in opposite directions in the region of mutual magnetic flux between the planes, thereby decreasing the total magnetic flux and the total inductance.) This mutual inductance can also increase the capacitor's effectiveness in reducing the PDN impedance and increase the maximum frequency for which this decoupling capacitor can be effective. A circuit representation of Figure 2 is shown in Figure 3.

The via pins connected to the same power layer (as seen in Figure 2) are coupled through an area of mutual magnetic flux, resulting in a mutual inductance. The mutual inductance is seen in the equivalent circuit representation of the power delivery network in Figure 3. This mutual inductance is a function of the IC/decoupling capacitor spacing (s), ground/power layer spacing, or thickness (d), and the proximity of both components to the edges of the board [2].

III. LOCAL DECOUPLING EFFECTS

Local decoupling as seen in the frequency domain

The mutual magnetic coupling (mutual inductance) between vias produces two distinct effects which are beneficial to decoupling:

- The series resonant frequency of the decoupling capacitor is increased. In other words, the frequency range over which the capacitor behaves as a capacitor is increased. The series resonant frequency of the capacitor is inversely proportional to the square root of the series inductance. As the loop area decreases with increasing proximity of the IC and capacitor, the inductance of the loop, L_{total} , decreases primarily due to the increasing mutual coupling (mutual inductance) between the vias, as indicated in Figure 2. (Figure 1 is a notional figure intended to illustrate an overview of the physics. In order to be more precise and consistent with published work, from this point forward, the inductance components are referred to as L_1 , L_2 and L_3 . L_1 and L_2 form L_{below} from the Figure 1. L_3 is the L_{above} term.)
- The power bus impedance is reduced uniformly in a fre-

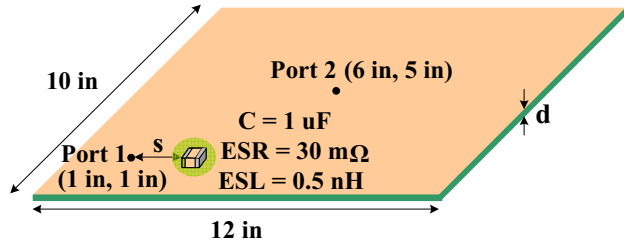


Figure 5: The power bus geometry consists of a PCB with a single moveable decoupling capacitor. Port 1 represents the location of an IC power pin and Port 2 allows observation of the power bus voltage as the local decoupling capacitor is moved. Power bus thicknesses of 35 mils and 10 mils are considered.

quency-independent manner for a wide range of frequencies higher than the series resonant frequency. (This is an approximate effect that is more valid when the power bus impedance is low than when it is high.)

These two important effects of mutual coupling between vias are illustrated in Figure 4, where the shifting of the series resonant frequency and the reduction of power bus impedance above that frequency are shown. At frequencies higher than the series resonant frequency of the capacitor, the decrease in power bus impedance can be approximately described by (2), which shows the reduction in the transfer impedance between two points on the power bus (approximate over a wide frequency range) [2].

$$|Z_{21}|_{decrease}(dB) \approx -20 \log_{10} \left[\frac{L_2(1-k) + L_3}{L_2 + L_3} \right] \quad (2)$$

$$= -20 \log_{10} \left[\frac{(1-k) + \left(\frac{L_3}{L_2}\right)}{1 + \left(\frac{L_3}{L_2}\right)} \right]$$

The critical terms are the mutual coupling coefficient, k , between the local decoupling capacitor and IC vias, and the ratio of the portion of the interconnect inductance above the planes, relative to that in the planes, L_3/L_2 . The portion of the inductance above the planes represented by L_3 is comprised of both the portion of the capacitor via above the power/ground plane pair, the interconnect trace, and the ESL of the capacitor. (In (2), the mutual inductance between the local decoupling capacitor via above the power planes and the IC interconnect above the planes is neglected. While this can easily be accounted for by splitting M into the two components, the mutual inductance between the planes is usually dominant. If it is not dominant, the ratio of L_3/L_2 is greater than one and little benefit from local decoupling can be achieved.)

The quantities employed in Equation (2) and described in Figures 2 and 3, i.e., k and L_3/L_2 , can be both calculated by means of analytical expressions [6, 7, 8]. The via inductances between the planes can be calculated from the equation

$$L_1 = L_2 = \frac{\mu_0 d}{2\pi} \left[\ln \left(\frac{R_{equiv}}{r} \right) - 0.75 \right] \text{ H} \quad (3)$$

where d is the plane spacing in meters, r is the radius of the via, and R_{equiv} is the radius of the power bus if it were circular. Since most PCB power buses are rectangular, this is the equivalent radius.

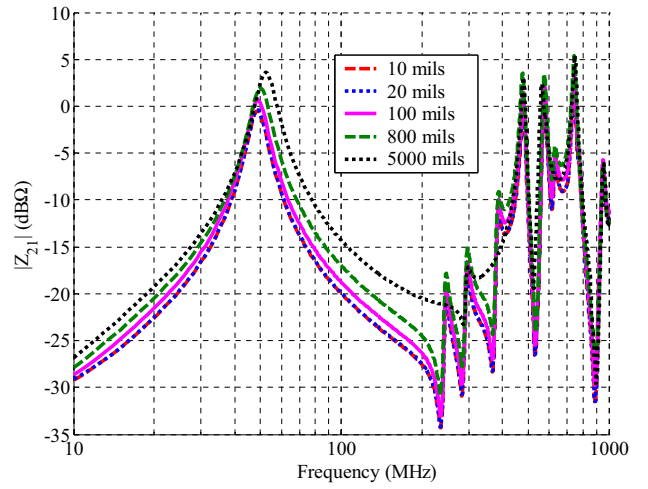


Figure 6: The transfer impedance between Ports 1 and 2 for different distances between Port 1 and the capacitor shows some decrease as the capacitor nears Port 1. The thickness of the parallel plate geometry is 10 mils.

For a rectangular power bus, R_{equiv} can be estimated from

$$R_{equiv} = \frac{a+b}{4}, \quad (4)$$

where a and b are the rectangular dimensions of the power bus.

L_3 is the inductance above the planes and consists of the interconnect inductance (pad and trace) and the ESL of the capacitor. The interconnect inductance portion of L_3 is not so easily calculated from a simple formula [9, see Appendix]. A small trace length between the pad and via can add significant inductance (this is demonstrated later). The limiting factors are often due to manufacturing issues at PCB fabrication and component assembly [10]. A practical lower limit on the interconnect inductance, L_3 , is probably on the order of 0.5 nH.

The dimensionless coupling coefficient, k , can be estimated from [8]:

$$k \approx \frac{\ln(R_{equiv}/(s+r)) - 0.75}{\ln(R_{equiv}/r) - 0.75} \quad (5)$$

where R_{equiv} is the equivalent radius of the board, s is the spacing between the decoupling capacitor and IC vias, and r is the via radius. The coupling coefficient, k , ranges in value between zero and unity.

As an example, Figure 5 illustrates a PCB configuration that is a rectangle of dimensions 10 x 12 inches. Port 1 simulates the location of a switching IC power pin. A movable decoupling capacitor is placed a distance, s , from Port 1. The capacitor has a value of 1 μF , an ESL of 0.5 nH, and an ESR of 0.03 Ω . Port 2 represents a somewhat random location at which the voltage of the power bus may be observed. SPICE models for the PCB in Figure 5 were extracted by means of a cavity model analysis tool with a circuit extraction feature [11, 12, 13]. This yields a lumped element model that includes the planes, ports and capacitors. The comparisons of the transfer impedance, $|Z_{21}|$, between Ports 1 and 2 for different capacitor distances from Port 1 are shown in Figures 6, 7 and 8, for frequencies up to 1 GHz and for separation distances between power and ground planes of 10 and 35 mils, respectively. In this figure, $L_3' = 0$, which is an exaggeratedly low value, but which accentuates the effect of the mutual coupling. (L_3' is the interconnection induc-

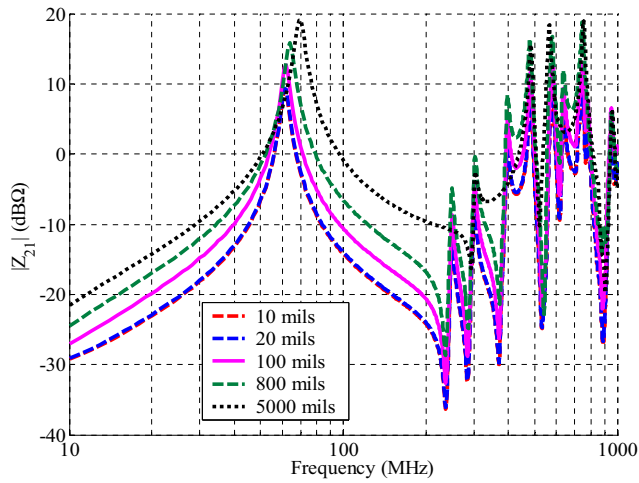


Figure 7: The transfer impedance between Ports 1 and 2 for different distances between Port 1 and the capacitor shows significant decrease as the capacitor nears Port 1. The thickness of the parallel plate geometry is 35 mils. A decrease in impedance of a few dB is seen as the capacitor is moved closer to Port 1. Data from this chart was used to create Figure 4.

tance of the capacitor above the power bus planes, excluding the ESL of the capacitor, as indicated in Figure 2.) The greater decreases in $|Z_{21}|$ in the 35 mil structure than in the 10 mil structure, imply that the 35 mil structure is better for supporting capacitor location dependent local decoupling. Thicker power bus structures inherently provide more mutual coupling between vias, hence, better support for local decoupling effects. While it is difficult to see in these figures, the decrease in $|Z_{21}|$ is seldom greater than a few dB for a single local decoupling capacitor. A change of 6 dB is an approximate upper bound of the impedance decrease for practical PCB stack-up dimensions, with a decrease of 3-4 dB being a more practical expectation [8].

Two factors play an important role in expression (2), i.e., the ratio L_3/L_2 and the coupling factor k . The decrease in $|Z_{21}|$ is negligible if the vias are so loosely coupled that there is no mutual coupling, or if L_3 is much greater than L_2 , i.e., the interconnect inductance of the via within the power/ground pair is much smaller than the sum of the interconnect inductance above the power/ground plane and the ESL. A relatively large ratio of L_3/L_2 is easily achieved when the distance between the power and the ground plane is small; therefore thin power/ground PDN's often receive few benefits from a local decoupling strategy.

Local decoupling as seen in the time domain

A different and possibly more intuitive way to examine PCB decoupling is to examine the phenomenon in the time domain. As discussed earlier, as an IC power pin switches very quickly from a high impedance state to a low impedance state (drawing current), the initial current must come from the portion of the power bus that is able to deliver charge in a nearly instantaneous manner. This part of the power bus is either a local decoupling capacitor or the stored charge between the power/ground-reference plane pair, or some combination of the two. In normal circumstances, as current is drawn from the power bus, some voltage drop occurs due to non-zero imped-

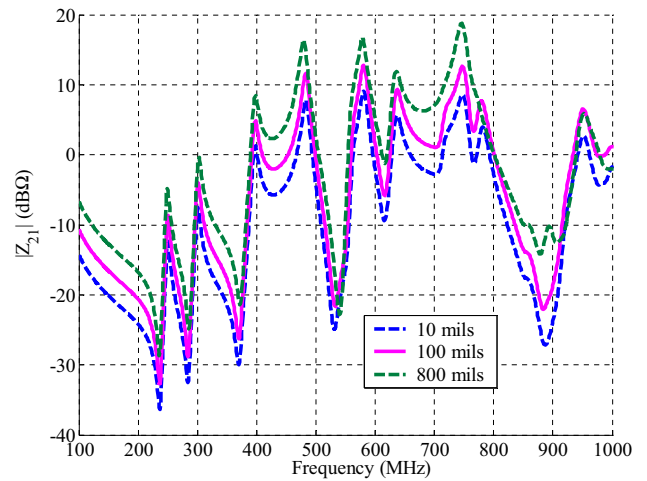


Figure 8: An extracted and expanded view of the data from Figure 7 on a linear scale better illustrates the decrease in transfer impedance in the high frequency range above the series resonant frequency of the capacitor.

ance of the power bus. If sufficient current is not available quickly enough from the decoupling capacitor (due to the inductance associated with the current path) then the voltage will dip more substantially, causing a noticeably higher ripple voltage and EMI 'noise'. As the decoupling capacitor is moved farther away from the IC, the inductance associated with any current from the capacitor increases, resulting in less current provided and a higher noise level.

It is worth noting that there is a perception in the design community that the IC power/ground pin pair represents a source of power bus noise that should be prevented from getting onto the PCB PDN. The IC has its own power bus with a non-zero impedance and non-instantaneously available charge sources, along with numerous transistors switching states at various rates. Therefore the IC, itself, suffers power bus noise. However, the PCB suffers power bus voltage ripple simply due to the switching of the IC power pin state (as it would if the IC power/ground pins were represented by a simple switch). Usually, the most important physics of PCB power bus decoupling is that of an IC power/ground pin switching states rapidly which demands current from either a local decoupling capacitor or the stored charge between the power/ground-reference plane pair, as discussed in this paper and [1].

Power bus thickness (mils)	via diameter (mils)	L_2 (nH)
10	10	0.32
10	13	0.304
10	25	0.27
35	10	1.1
35	13	1.07
35	25	0.95

Table 1: Calculated values of the inductance of the vias between the planes in a power bus for two common power bus thicknesses and common values of via diameter.

To examine decoupling from the perspective of the time domain, the PCB configuration from Figure 5 is re-examined. The simulated IC power pin, represented by Port 1, is represented by a time-dependent current source. This may not be the highest fidelity simulation of the switching power pin, but it is sufficiently accurate to be illustrative. In this case, the current source is a pulse with an isosceles triangular shape that has 2 ns duration with the peak reached at 1 ns, as seen in Figure 9.

Figure 10 shows the resulting voltage at Port 2 versus time for various decoupling capacitor locations. The voltage waveforms shown are for the case of a power bus thickness of 35 mils and $L_3' = 0$ (no interconnect inductance), an ESL value of 0.5 nH, and an ESR of 0.03 Ohms. The lack of interconnect inductance is unrealistic and exaggerates the effect of capacitor location but is used in this figure for illustrative purposes. The voltage peak at Port 2 during the first cycle of disturbance is much greater when the local decoupling capacitor is very far from Port 1 than it is when the capacitor is close to Port 1. This demonstrates that the location of the capacitor is important in determining the voltage swing, ripple voltage, at Port 2 as a result of state changes at Port 1. The initial cycle of the voltage disturbance is the time period during which the IC is in most need of rapidly delivered charge. The smaller voltage swing during the initial disturbance when the decoupling capacitor is located close to the IC (s is small) is indication that the IC's initial thirst for charge is more easily satisfied when the capacitor is close to the IC pin than when it is far away. This is consistent with the previous discussion. The values of the coupling coefficient, k , are noted for each value of distance between the vias.

Note that the waveform of the source current seen in Figure 9 begins its rise approximately 1 ns earlier than the rise in voltage at Port 2 that is seen in Figure 10. This is consistent with the propagation time over the distance between Ports 1 and 2.

The thirst for charge during the initial cycle of disturbance is important to the functionality of the IC. This time dependency of the voltage disturbance that comprises the power bus ripple is not so intuitively apparent when examining decoupling in the frequency domain [14]. It should also be noted that although the power bus planes and decoupling capacitor values and locations may be designed to supply charge to the IC and lower the power bus impedance, it can also be simultaneously true that insufficient charge is available to meet the demand of a particularly charge-thirsty IC. In this case, functional difficulties may result as the device may experience output waveform distortion. This is a topic beyond the scope of this paper.

Figure 11 shows the change in peak voltage, ΔV_p , in this initial disturbance period at Port 2 vs. distance between the capacitor and Port 1 (simulated IC power pin) from the power bus configuration shown in Figure 5. ΔV_p uses the voltage at Port 2 when the capacitor is located far away ($s = 5000$ mils, $k = 0$) as a reference. Thus, a negative value of ΔV_p indicates a lower voltage at Port 2 due to presence of the local capacitor than when the capacitor is far away. The capacitor has an ESL of 0.5 nH and an ESR of 0.03 Ohms. A larger absolute value change in peak voltage indicates a larger dependency on location of the capacitor. From Figure 11, it is clear that for the thicker power bus, $d = 35$ mils, the power bus voltage at Port 2 has a greater dependency on the proximity of the decoupling capacitor than the thinner power bus ($d = 10$ mils). Figure 11 also shows that the interconnect inductance is an important fac-

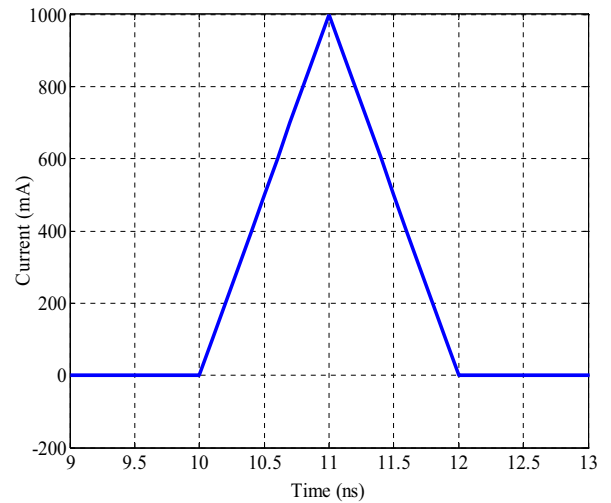


Figure 9: A triangularly shaped current source with a time to peak of 1 ns is applied to Port 1 to simulate an IC power pin that switches states.

tor in the local decoupling effect. The dashed lines in Figure 11 show the peak location-dependent change in voltage when the interconnect inductance above the power bus (L_3') is 1 nH is less (>100 mV for $s < .8$ inches for the 35 mil power bus) than when the interconnect inductance is zero.

IV. DESIGN IMPLICATIONS

L_2 , L_3 and k are important parameters in determining the potential for local decoupling behavior. Their values depend on the specifics of particular PCB stack-ups and layouts. Nevertheless, some typical values may be estimated for discussion. L_2 is calculated from Equation (3). For a PCB that has dimensions of 10 x 12 inches, similar to that shown in Figure 5, Table 1 shows values for L_2 for some typical values of via diameter. The value of L_2 does not depend on the placement of the power bus in the overall stack-up, whereas L_3' does.

The coupling coefficient, k , is indicated on Figure 10 for various distances between capacitor and IC vias. This is calculated from Equation (5) and is only a function of via spacing and board size, not stack-up.

The ratio L_3/L_2 is a good indicator of the ability of a decoupled power bus to support local decoupling. While many factors can enter into the efficiency of local decoupling, the lower the

centered power bus thickness (mils)	L_3' (nH)	L_3/L_2	L_3/L_2 w/extra 100 mil trace length	L_3/L_2 w/extra 200 mil trace length	L_3/L_2 w/extra 300 mil trace length
10	1.66	6.75	9.13	11.50	13.88
35	0.92	1.29	1.98	2.67	3.36

Table 2: Values of L_3 interconnect inductances for power buses centered in the stack-up, 10 mil via diameters, 0603 capacitor pads and showing the effects of even small extra trace lengths connecting vias and pads.

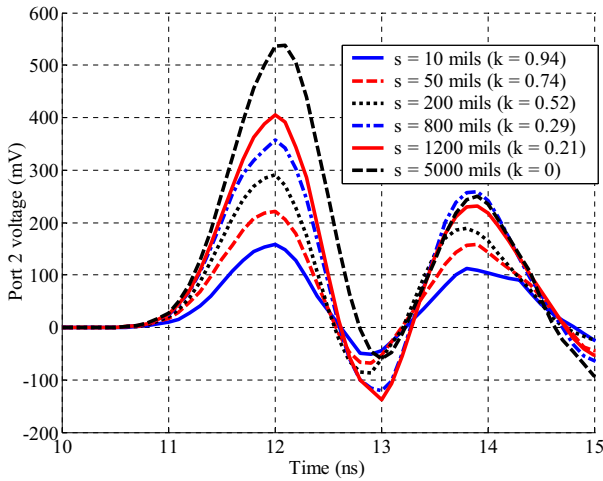


Figure 10: The voltage vs. time measured at Port 2 due to the current source from Figure 9 applied to Port 1. The power bus thickness is 35 mils.

ratio L_3/L_2 , the more likely that effective local decoupling may be achieved. As a general rule of thumb, the ratio of L_3/L_2 should be approximately 3, or lower, to achieve significant local decoupling. Note that this rule of thumb may not be valid for specific PCB configurations. Also, note that L_3 includes the ESL of the capacitor, which can vary among capacitors of the same package size.

L_3 is even more dependent on specifics of layout and not so simply calculated. Table 2 shows inductance values for power buses that are centered in the PCB stack-up for a 62 mil finished PCB thickness. The tabular values are derived using engineering estimates of the contributions of inductance of via lengths from a power bus centered in a PCB stack-up for a PCB of 0.62 inch finished thickness, and surface solder pads for an 0603 SMT capacitor. Table 2 also shows the effects of even very short extra lengths of microstrip trace to connect vias to pads. The ratio L_3/L_2 is quite large in the case of the 10 mil power bus reflecting the earlier conclusion that it is difficult to achieve local decoupling behavior with a thin power bus in a 0.062 inch

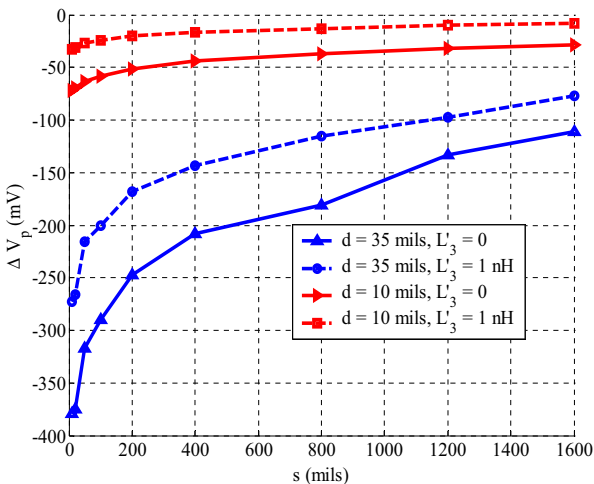


Figure 11: The change in peak voltage at Port 2, due to a switching current at Port 1, versus distance between the capacitor and Port 1. Values are referenced to the peak voltage when $s=5000$ mils (far away).

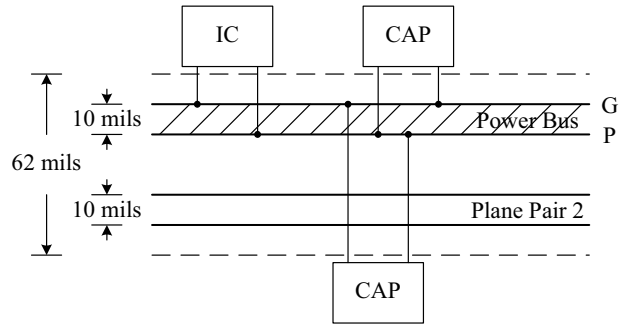


Figure 12: When power buses are moved away from the center of the stack-up, the L_3/L_2 inductance ratios are asymmetric and depend greatly on the surface on which the decoupling capacitor is placed.

PCB configuration. A thinner finished board thickness will lower the ratio and increase the ability of the PCB to support local decoupling. On the other hand, the 35 mil power bus exhibits a ratio L_3/L_2 of only a little higher than 3 even with an extra 300 mil trace length. Clearly, the thicker power bus in a 0.062 inch PCB is amenable to local decoupling.

Table 3 shows interesting effects when the power bus is not centered in the PCB stack-up as shown in Figure 12. When positioning a power bus off-center in the stack-up, two power buses must be used in order to maintain PCB symmetry, or at least an identical two plane structure. It is, therefore, impossible to use two 35 mil power buses in a PCB with a finished thickness of 62 mils. The figure shows a PCB with two power buses, each with a thickness of 10 mils. The IC is mounted on the obverse surface of the PCB with decoupling capacitors mounted on either observe or reverse sides of the board. The table shows the effects of moving a 10 mil power bus near the obverse surface of the PCB in terms of the L_3/L_2 ratio. The decoupling capacitor on the obverse surface of the PCB has relatively short via lengths that form L_3' . The capacitor on the reverse side requires relatively long via lengths to reach the power bus connected to the IC. Table 3 shows that the ratios of L_3/L_2 are vastly different depending on the surface upon which the capacitor is mounted. A capacitor ESL value of 0.5 nH was used when calculating L_3 . When the capacitor is mounted on the obverse surface L_3/L_2 is less than three, indicating the potential for effective local decoupling. However, when the capacitor is mounted on the reverse surface, L_3/L_2 is greater than nine, indicating slim possibility of effective local decoupling. Hence, the position of the power bus in the PCB stack-up, along with

DeCap Placement	L3' (nH)	L3/L2
Obverse	0.45	2.96875
Reverse	2.56	9.5625

Table 3: Interconnect inductances associated with capacitor connections to a 10 mil power bus that is off-centered in the PCB stack-up, near the obverse side of the PCB. Capacitor ESL= 0.5 nH.

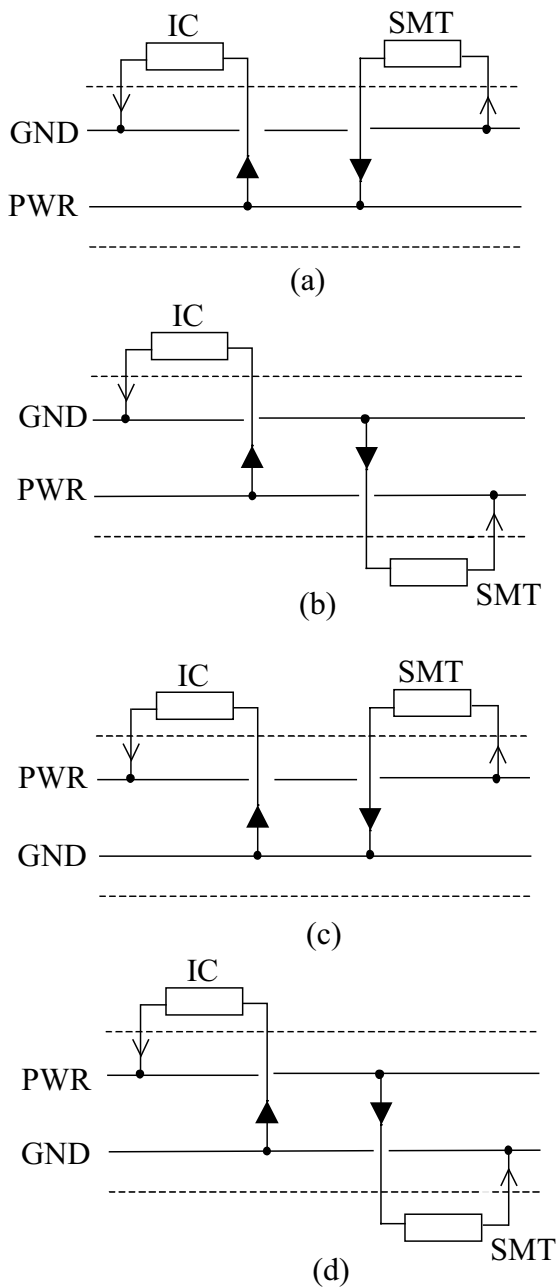


Figure 13: Examples of effective placement of SMT decoupling capacitors and proximate IC power/ground pins on a PCB power bus. The close proximity of the longer via lengths increases the mutual coupling between the vias and enhances local decoupling behavior.

placement of the capacitor can be very important in achieving effective local decoupling.

Figure 13 shows the proper ways to place SMT decoupling capacitors near IC power pins in order to increase the mutual inductance between capacitor and IC vias, hence to take best advantage of local decoupling behavior. The four examples include all combinations of capacitors on top or bottom and power plane above or below the ground plane. (The terminology “top” and “bottom” refer to the obverse and reverse sides of the PCB, which is often characterized by layer numbers in the PCB stack-up, layer 1 is near the top, etc.). The conclusion is

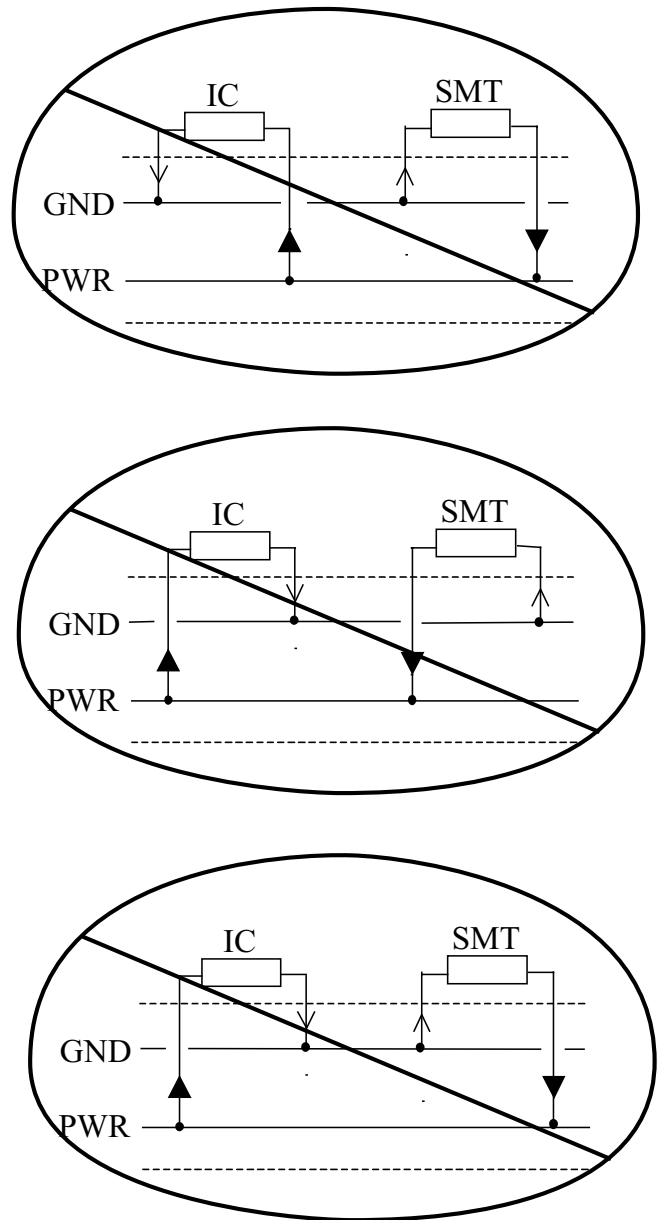


Figure 14: Examples of the three incorrect combinations of placement of IC and capacitor, corresponding to Figure 13(a). Each of the remaining three “right” configurations in Figure 13 have three “wrong” configurations that can be deduced from this figure.

that the IC power or ground pin and SMT capacitor should be placed so that the longer vias are proximate. This increases the mutual coupling and gives greatest weight to local decoupling behavior [2].

Figure 14 shows the “wrong” ways that one could place the decoupling capacitor, corresponding to Figure 13(a). From this one can extrapolate the configurations shown in Figures 13(b-d) to obtain the “wrong” ways to place the decoupling capacitor in those configurations. The rule is that if the longer vias are not proximate, the placement is wrong in the sense that the mutual inductance between the vias is not maximized; hence the potential for local decoupling is not maximized [2].

In practice, PCBs that require decoupling have several layers

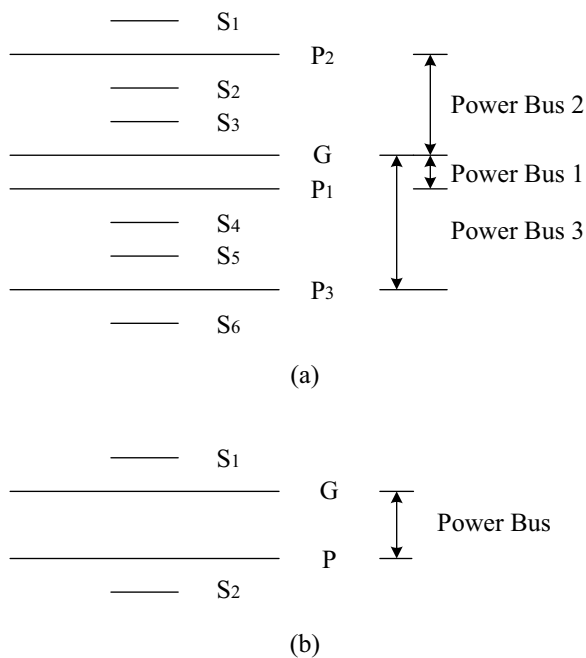


Figure 15: Typical PCB stack-ups illustrating how various power bus structures may be formed in a single PCB of 62 mil thickness: (a) a 10-layer stack-up; (b) a 4-layer stack-up.

that usually include multiple reference planes that form more than one power and/or ground planes. These PCB structures will exhibit more than a single power bus structure. As an example, a representative 10-layer PCB stack-up for a PCB with a finished thickness of 62 mils with three power planes, one ground plane and six signal layers is illustrated in Figure 15(a). Power Bus #1 may typically have a thickness of 10 mils or less and should offer superior decoupling opportunity, but will not be very effective in supporting local decoupling. From the previous discussion, the ratio of L_3/L_2 may be on the order of seven in the most favorable configuration. Hence, a designer would expect that all decoupling capacitors associated with Power Bus #1 would act globally. Power Bus #2 may have a thickness on the order of 20 mils. Therefore, Power Bus #2 will be more amenable to local decoupling behavior, since the L_3/L_2 ratio is probably much lower. Power Bus #3, which has a thickness on the order of 30 mils, is an unconventional power bus structure in that it contains three planes, but this is actually a very common configuration. Its decoupling behavior should be similar to that of a 30 mil power bus, but there may be some small differences in the values of the inductances and the mutual coupling due to the presence of the extra reference plane. This power bus may also provide opportunities for most local decoupling effects, but may be most effective with capacitors mounted on the reverse side of the PCB.

Figure 15(b) shows a simpler 4-layer PCB stack-up with a single power plane and a single ground plane. For a finished board thickness of 62 mils, the power bus may have a thickness close to the 35 mil thickness that has been discussed in this paper. In this case, as we have seen in examples in this paper, effective local decoupling can be supported provided that the layout is done in a manner that keeps the ratio of L_3/L_2 suffi-

ciently low and the coupling coefficient, k , is maintained sufficiently high.

So, how close must a decoupling capacitor be to the IC pin to achieve effective local decoupling? No simple answer can be given to this question because the performance of a local decoupling capacitor depends on the power bus thickness, d , the inductance ratio, L_3/L_2 , and the IC/capacitor spacing, s . As a rule of thumb, however, for a 35 mil thick power bus structure with a favorable L_3/L_2 ratio (3, or less), a 3 dB decrease in both port voltage and power bus transfer impedance requires a capacitor to be within approximately 200 mils, or less of the IC power/ground pin. This is very close. Indeed, for some IC devices such as BGA packages, it may not be practical to place a capacitor that close to a solder ball. But, note from Figure 11 that there is an effect on port voltage even as far out as 1600 mils (no data is shown beyond that). Therefore, if a designer intends to make the best use possible of the increased decoupling effects of local decoupling and the inductance ratio is favorable, a capacitor may be placed as close as possible and some local decoupling effect will be achieved, even if it is less than the 3 dB used as a benchmark above. For the case of a 10 mil power bus thickness with the same favorable L_3/L_2 ratio, it is virtually impossible to achieve a 3 dB change in port voltage or decrease in transfer impedance. Note that if a lower inductance ratio is achieved, the 3 dB reduction in voltage and impedance can be achieved with capacitors placed farther from the IC power/ground pin. Aggressive power bus designs can achieve lower L_3/L_2 ratios by attention to detail in designing for very low interconnect inductances through careful part placement and solder pad design.

Regarding 10 mil power bus structures, the 3 dB benchmark local decoupling effect may be achieved if the power bus is located near one of the surfaces of the PCB stack-up, similar to that seen in Figure 12.

In today's design climate that emphasizes PCB density, many PCB stack-up designs provide for one or more voltage planes to be split so that the layer can support two or more different voltages. This is usually done to maintain a desired density on the PCB without incurring the cost of adding additional power plane layers. How, then, does this affect the way in which decoupling should be designed? Generally speaking, using split voltage planes does not substantially affect decoupling, either local or global decoupling behavior. The values of the interconnect inductances and the mutual coupling coefficient may undergo some change if only a partial plane is used in the decoupling circuit, but those changes are probably minor. The exception may be if only a very small power island is used for a particular voltage, the changes to parameter values may be more significant.

V. CONCLUSIONS

In general, PCB power bus structures that have little thickness (<10 mil) provide superior decoupling. However, thicker power bus structures offer better opportunities for location-dependent decoupling, i.e., capacitors that behave locally, rather than globally.

Responsiveness of the decoupling capacitor is the key to achieving effective location-dependent decoupling. This means that the inductance of the interconnect circuit should be minimized.

Most decoupling capacitors on today's multi-layered PCB behave globally in that the specific location of the capacitor does not significantly affect the voltage on the power bus. Mutual magnetic coupling between the IC and decoupling capacitor's vias increases the likelihood that the proximity of the IC power pin and decoupling capacitor can be significant. The local decoupling effect that is enabled by mutual coupling between vias is manifested by an increase in the series resonant frequency of the particular decoupling capacitor and a decrease in the power bus impedance at frequencies above the series resonance of the capacitor, resulting in decreased voltage fluctuations on the power bus. Without carefully designed SMT capacitor solder pads, or trace connections from pad to via, the "above the plane" interconnect inductances may be increased sufficiently so that local decoupling effects are not significant, even on thick

power bus structures. When constrained to common PCB finished thicknesses (such as 62 mils), multilayered PCBs with many layers and multiple planes will not have power bus structures with sufficient thickness to support many opportunities for local decoupling.

Simpler PCBs, such as 4-layer stack-ups with standard finished thicknesses are more amenable to local decoupling behavior. Successful implementation of local decoupling depends greatly on the details of the layout of the interconnection between both the IC and capacitor's connections to power and ground planes.

The next paper in this series will discuss design issues related to the reference planes (power, ground) and PCB laminate materials in the multi-layered PCB stack-up and how they influence decoupling.

VI. APPENDIX

The following equations from [9] provide a closed form method for calculating L_3^1 .

$$M_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[\frac{h_s}{s} + \sqrt{1 + \left(\frac{h_s}{s}\right)^2} \right] + \frac{s}{h_s} - \sqrt{1 + \left(\frac{s}{h_s}\right)^2} \right\} \quad (\text{A1a})$$

$$L_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[\frac{h_s}{r} + \sqrt{1 + \left(\frac{h_s}{r}\right)^2} \right] + \frac{r}{h_s} - \sqrt{1 + \left(\frac{r}{h_s}\right)^2} \right\} \quad (\text{A1b})$$

$$L_{via} = 2(L_{ps} - M_{ps}) \quad (\text{A1c})$$

$$M_t = \frac{10^{-7}}{w^2} \left[\begin{aligned} & -\frac{2}{3} (w^2 - 2p^2 + s^2) \sqrt{w^2 + p^2 + s^2} \\ & + s(w^2 - p^2) \ln \left(\frac{s + \sqrt{w^2 + p^2 + s^2}}{-s + \sqrt{w^2 + p^2 + s^2}} \right) \\ & + \frac{2}{3} (w^2 - 2p^2) \sqrt{w^2 + p^2} \\ & + s^2 w \ln \left(\frac{w + \sqrt{w^2 + p^2 + s^2}}{-w + \sqrt{w^2 + p^2 + s^2}} \right) \\ & - 4wps \tan^{-1} \left(\frac{ws}{p\sqrt{w^2 + p^2 + s^2}} \right) \\ & + \frac{2}{3} (s^2 - 2p^2) \sqrt{s^2 + p^2} \\ & + p^2 s \ln \left(\frac{s + \sqrt{s^2 + p^2}}{-s + \sqrt{s^2 + p^2}} \right) + \frac{4p^3}{3} \end{aligned} \right] \quad (\text{A2a})$$

$$L_i = \frac{2 \times 10^{-7}}{3w^2} \left[3w^2 s \ln \left(\frac{s + \sqrt{w^2 + s^2}}{w} \right) + 3s^2 w \ln \left(\frac{w + \sqrt{w^2 + s^2}}{s} \right) \right] - (w^2 + s^2)^{3/2} + s^3 + w^3 \quad (A2b)$$

$$L_{trace} = L_i - M_i \quad (A2c)$$

$$L_3' = L_{via} + L_{trace} \quad (A3)$$

where

s — separation between two vias

b_s — height of the capacitor from the nearest power or ground plane

w — width of the trace connecting two vias, or width of the capacitor package if no trace

r — radius of the via

p — $2b_s$

* For all the equations above, the dimensions are in meters, and the inductances are in Henrys.

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Biographies



James L. Knighten (S'62-M'77-SM'97) received his B.S. and M.S. degrees in electrical engineering from Louisiana State University in 1965 and 1968, respectively, and his Ph.D. degree in electrical engineering from Iowa State University in 1976. He is employed by the Teradata Division of NCR Corporation in San Diego, CA where he works on EMI, and signal integrity design and testing of high-speed digital signal transmission systems in massively parallel processing computing systems. Prior to joining NCR, he worked for Maxwell Technologies, Inc., where he was engaged in the design of hardened electronic systems against the effects of the electromagnetic pulse created by nuclear weapon detonation, EMI, lightning, and high-powered microwaves on electronic systems.

He has authored numerous technical papers on topics involving various aspects of electromagnetics and taught short courses on electromagnetic pulse effects and electronics survivability both in the USA and in Europe. He is a member of the IEEE EMC Society.



Bruce Archambeault (M'85-SM'99-F'06) is a Senior Technical Staff Member at IBM in Research Triangle Park, NC. He received his B.S.E.E degree from the University of New Hampshire in 1977 and his M.S.E.E degree from Northeastern University in 1981. He received his Ph.D. from the University of New Hampshire in 1997. His doctoral research was in the area of computational electromagnetics applied to real-world EMC problems. Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is currently a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society (ACES). He has served as a past IEEE/EMCS Distinguished Lecturer. He is the author of the book "PCB Design for Real-World EMI Control" and the lead author of the book titled "EMI/EMC Computational Modeling Handbook."



Jun Fan (S'97-M'00) received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. He currently is an employee of the Teradata division of NCR Corporation in San Diego, CA, and serves as a Senior Hardware Engineer. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power bus modeling, PCB noise reduction, differential signal-

ing, and cable/connector designs. He received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000.



Giuseppe Selli (S'00) received his Laurea degree from the University of Rome "La Sapienza" in June 2000. In January 2002, he joined the Electromagnetic Compatibility research group at the University of Missouri Rolla and he received his Master of Science Degree in Electrical Engineering in November 2003 with a thesis on "Time domain extrapolation and evaluation of surface-mount component parasitic inductance." He is a Ph.D. Candidate at the Electrical Engineering Department of the University Missouri-Rolla within the EMC Laboratory and he is currently at the IBM T.J. Watson Research Center on a co-op program within the High Speed Electrical/Optical Packaging Department. His research interests include signal and power integrity issues.



Liang Xue (S'06) received his B.S. degree in Electrical Engineering from Tsinghua University, Beijing, China, in 2003, and is currently pursuing the M.S. degree in Electrical Engineering at the University of Missouri-Rolla. He is a graduate research assistant in the Electromagnetic Compatibility Laboratory, University of Missouri-Rolla. His main research interests are in the area of signal integrity and power integrity.



Sam Connor (M'05) received his BSEE from the University of Notre Dame in 1994. He currently works at IBM in Research Triangle Park, NC, where he is a senior engineer responsible for the development of EMC and SI analysis tools/applications. Mr. Connor has co-authored several papers on computational electromagnetics, mostly applied to decoupling and high-speed signaling issues in PCB designs.



James L. Drewniak (S'85-M'90-SM'01) received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1985, 1987, and 1991, respectively. He joined the Electrical Engineering Department at the University of Missouri-Rolla in 1991 where he is one of the principle faculty in the Electromagnetic Compatibility Laboratory. His research and teaching interests include electromagnetic compatibility in high-speed digital and mixed signal designs, electronic packaging, and electromagnetic compatibility in power electronic based systems. **EMC**

Editor's Note: These authors are proud of their IEEE membership! In this second paper of their multi-part series, the authors have updated their biographies to add their IEEE membership status. For example, "S" refers to Student Member, "M" refers to Member, "SM" refers to Senior Member, and "F" refers to Fellow Grade Member. Congratulations to Bruce Archambeault for adding the "F" in this issue!