Design and Process Guidelines for Use of Ceramic Chip Capacitors

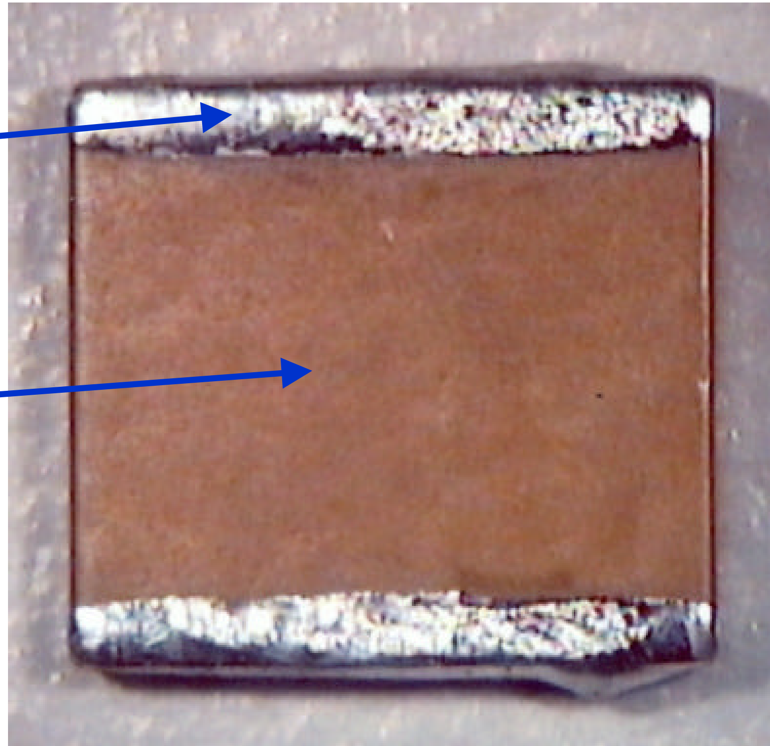
What are ceramic chip capacitors?

- Introduced in 1977
- Also known as multilayer ceramic capacitors (MLCC's)
- One of the most common components in the electronics industry
  - The largest manufacturers produce approximately 2 billion MLCC's per year
  - 98% yield would result in 40 million defective components
- Operating Specifications
  - 1 pF to 30 μF; 10 to 3000 volts

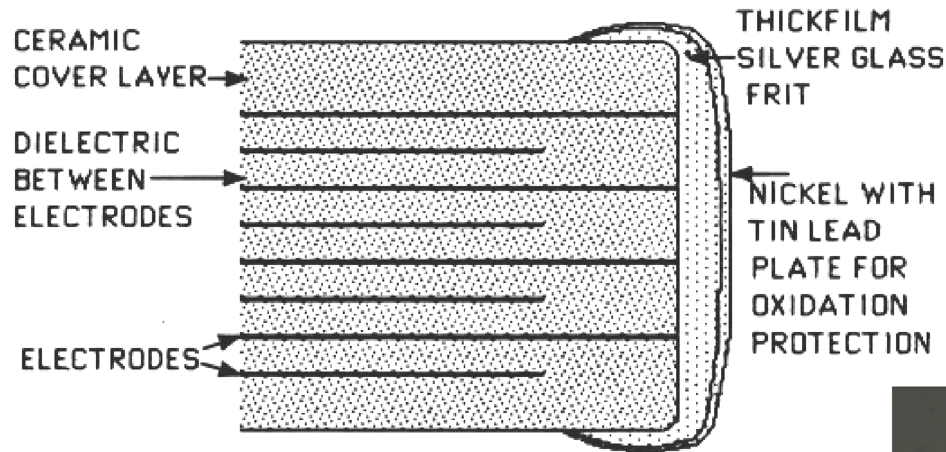
MLCC's

Termination/End Cap

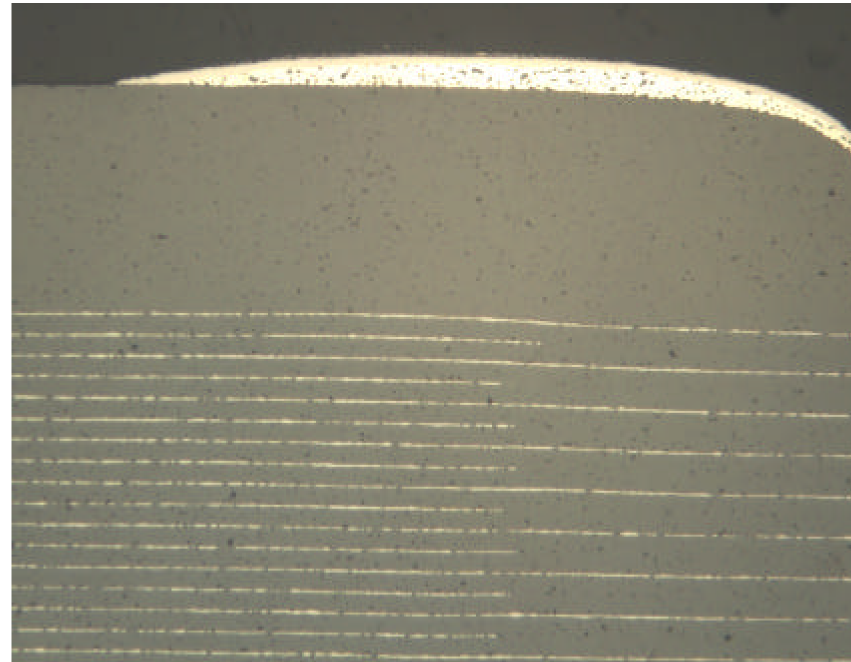
Body



Architecture of MLCC's



- Dielectric is a proprietary alloy of barium titanate
- Electrode is often an alloy of silver or silver palladium (rarer due to cost)
- Electrode spacing can be as small as 25 µm



Manufacture of MLCC's

- Two processes
  - Dry Sheet
  - Wet Build Up
- Final steps are similar
  - Termination:
    - Silver or silver palladium alloy frit
    - Nickel barrier layer
    - Tin overplate
  - 100% Final Testing
    - Insulation Resistance, Overvoltage (2x rated voltage), Capacitance and Dissipation Factor

Dry Sheet Fabrication

- Dry Build is most common
- Green tape process
  - Mixture of dielectric powder and organic binder
- Green tape is coated with a film of silver or silver palladium alloy
- The coated tapes are then stacked, pressed and the entire structure is sintered at 1000 to 1400°C.
- The dense blocks are then cut to final dimensions and tumbled to round corners
- Primary advantage: Tight control of electrode spacing

Wet Build Up Fabrication

- Uses screen printing to lay down successive layers of dielectric (ceramic) and electrodes
- Preform is cut and then baked to provide some degree of strength
- Rounding is followed by sintering to full density
- Process is closed-loop, fully-automated
  - Allows greater control with minimal handling
- Primary advantages:
  - High density of the wet layers reduces shrinkage
  - Wet process tends to induce better interlayer bonding

Manufacture of MLCC's (cont.)

- Standard sizes
  - 0805: 0.08 in x 0.05 in x 0.05 in (varies w/capacitance)
    2.0 mm x 1.3 mm x 1.3 mm
  - 0402, 0603, 1206, 1210, 1812, 1825, and 2225 (precludes high voltage)
  - 0201 starting to be introduced
- High volume manufacturers of MLCC's
  - Kemet ($1.4 billion in annual revenue)
  - AVX ($2.6 billion)(division of Kyocera)
  - Vishay ($2.4 billion)
  - Others: Murata ($3.1 billion, Japan), KOA-Speer, Sierra-KD, Rohm ($2.7 billion, Japan), TDK ($4.2 billion, Japan), Panasonic, and Phycomp (formerly Philips)

Failure of MLCC's

- Definitions
  - Failure Mode: The effect by which the failure is observed (i.e., capacitor burns)
  - Failure Mechanism: The process(es) by which the failure mode is induced (i.e., migration of silver between adjacent electrodes)
  - Failure Site: The physical location of the failure mechanism (i.e., board side of the termination of the end cap)
  - Root Cause: The process, design and/or environmental stress that initiated the failure mechanism (i.e., excessive flexure of the board)

Definitions (cont.)

- Definitions (cont):
  - Wearout Failures: Failures due to the accumulation of damage exceeding the endurance limit of the material
  - Overstress Failures: Catastrophic failures due to a single occurrence of a stress event
  - Intrinsic Defects: Defects introduced as a result of the raw materials or the manufacturing process
  - Extrinsic Defects: Defects introduced after the manufacture of the product

Do MLCC's Wearout?

- The primary type of mechanisms that induces wearout failures in MLCC’s is punch-through, which is an iterative process:
  - Areas of current leakage experience self-heating.
  - Causes deterioration of the insulation resistance
  - Leads to increase the current leakage
  - Eventually, a conductive path is formed between adjacent electrodes.
- Does not include failure of the solder interconnect, a common failure mode in large MLCC’s in severe environments.
  - Large, leadless, ceramic (small CTE)

MLCC Wearout (cont.)

- Due to the widespread practice of derating (operating the capacitor at 50% rated voltage) MLCC's are not expected to experience wearout during operation.
- According to Mogilevsky and Shin (1988):

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^3 \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

where t is time, V is voltage, T is temperature (K), E_a is an activation energy (~1.3) and K_B is Boltzman's constant (8.62×10^{-5} eV/K)

Operating Life

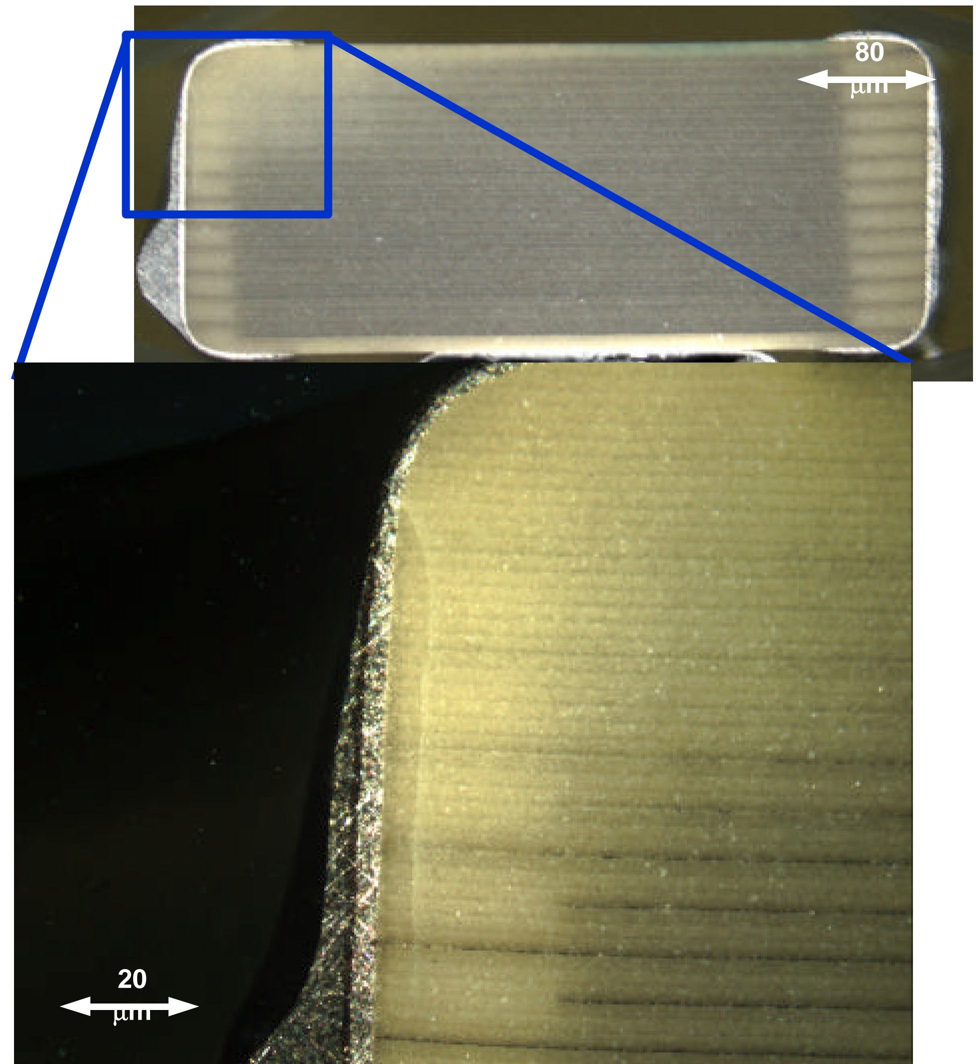
- Time to 1% failure ($t_{1\%}$) for a 50 volt MLCC is ~10 hours at 200 V and 200^oC
- Equivalent to ~100 years operating at 25 volts at 25^oC
- More recent work published by Kemet (Rawal, Krishnamani and Maxwell) suggest a higher activation energy (1.8 to 1.9)
  - Extends theoretical lifetime to 350 to 700 years

Intrinsic Defects

- The overwhelming percentage of MLCC's fail due to the introduction of intrinsic and extrinsic defects
- Intrinsic Defects (manufacturing)
  - Firing Cracks
  - Knitline Cracks (Delamination)
  - Voiding

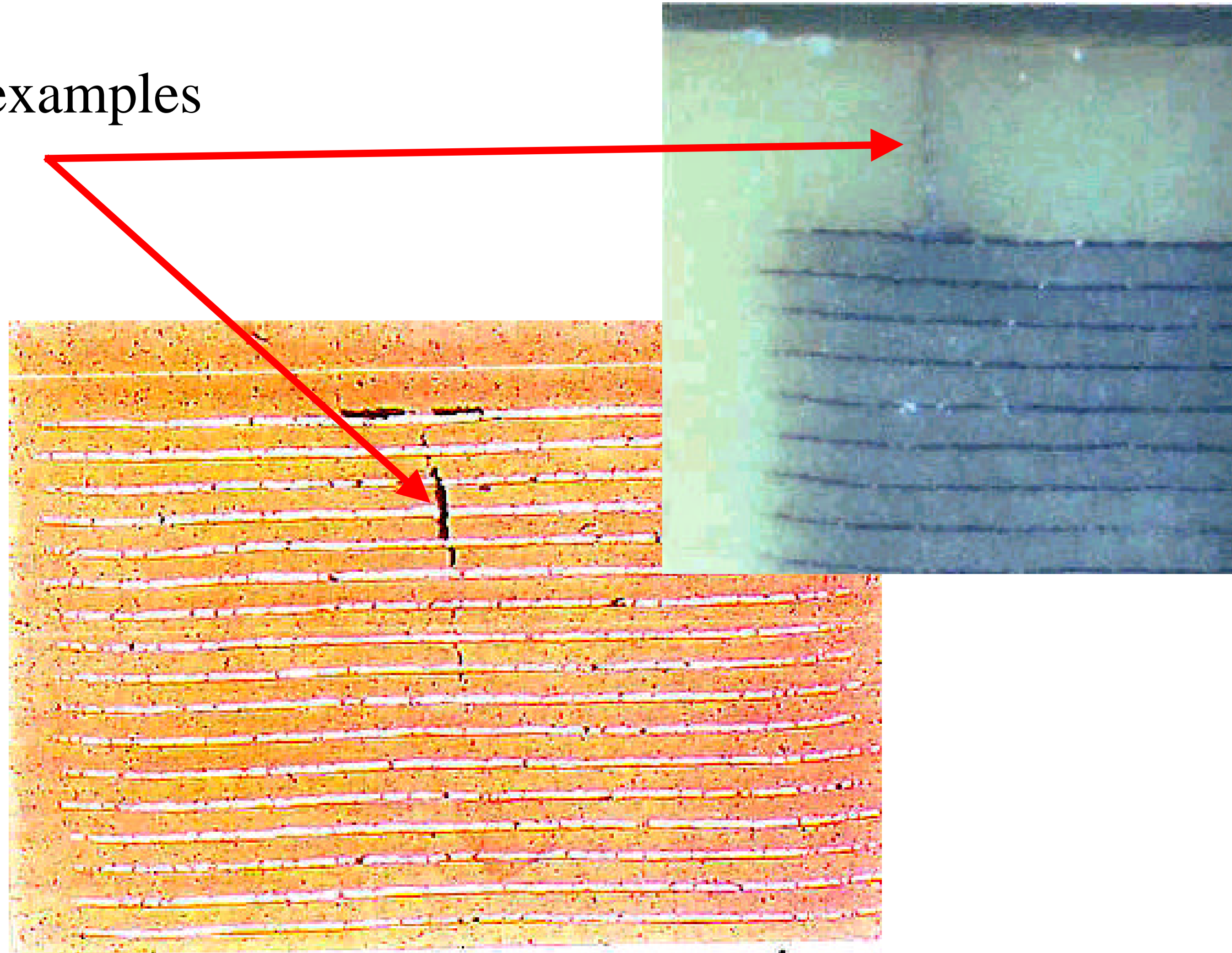
Firing Cracks

- Often originate at an electrode edge, but not always.
- Propagation path is perpendicular to the electrodes
- Root cause
  - Rapid cooling during capacitor manufacturing



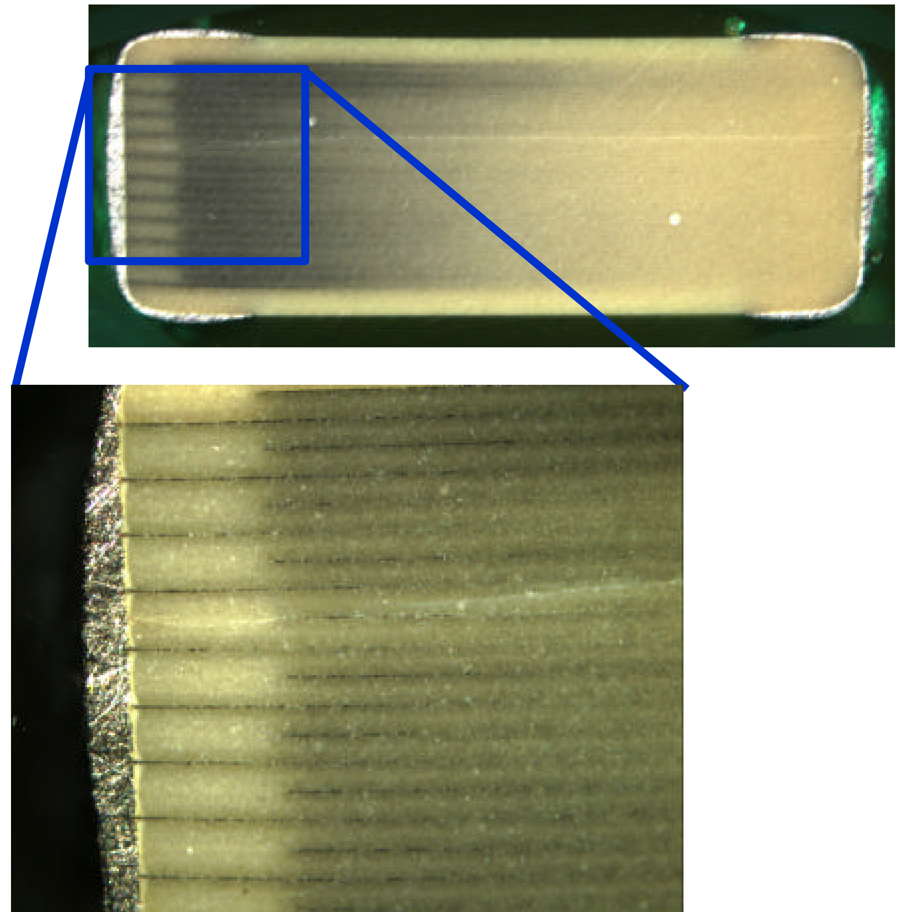
Firing Cracks (cont.)

Additional examples

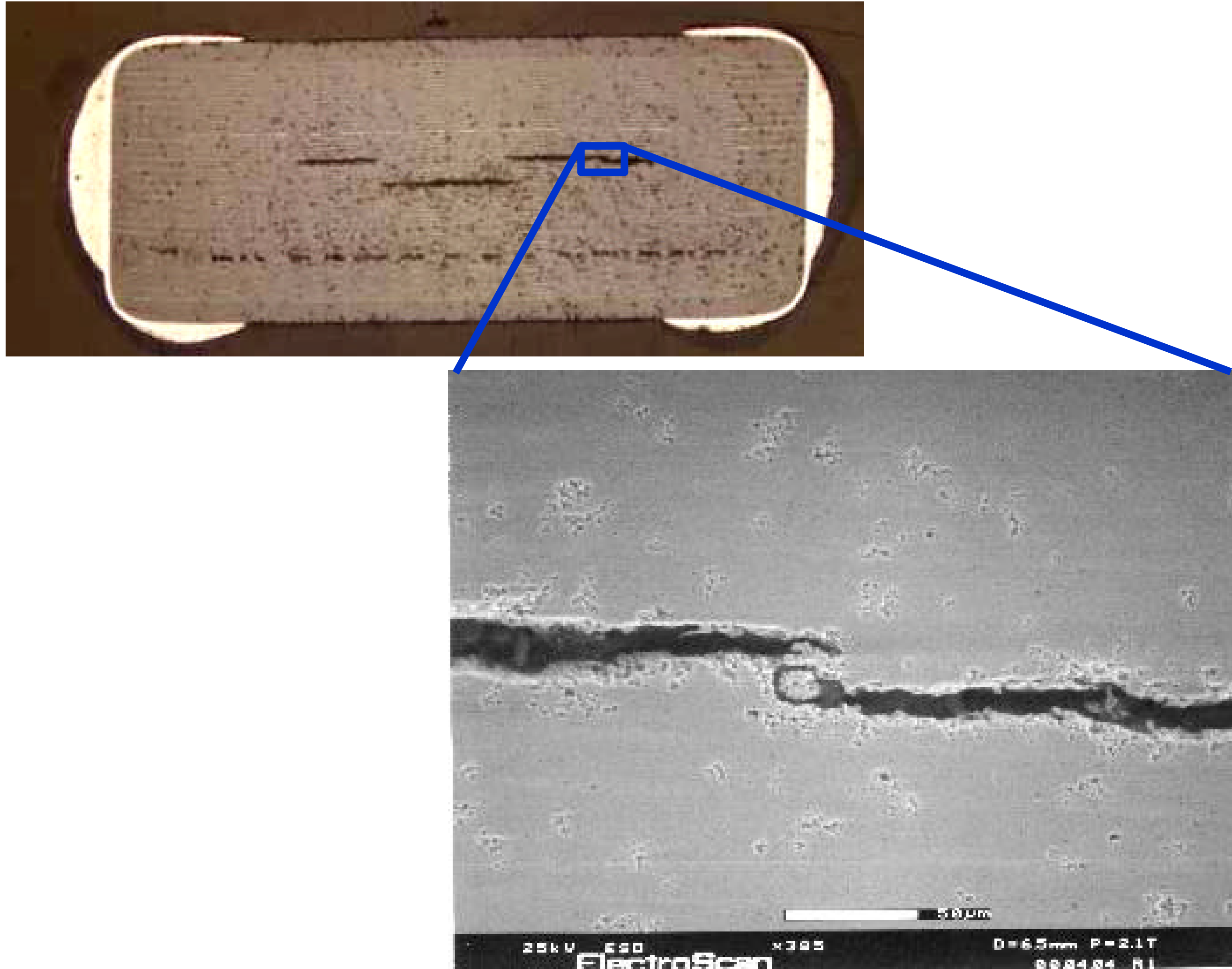


Knit Line Cracks

- Knit line cracks extend parallel to the electrodes
- Occur post-densification
  - Large crack openings
  - Jagged propagation paths
- Root causes
  - Non-optimized pressing or sintering
    - •Insufficient binding strength/Delamination
    - •Trapping of air or foreign material
    - •Internal sublimation of burnout material

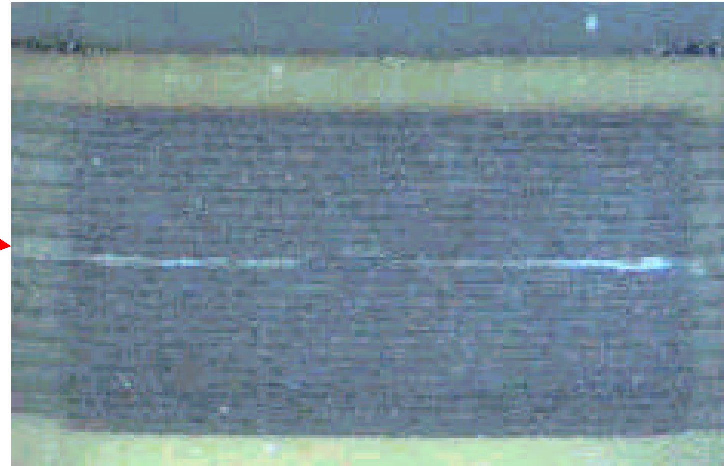


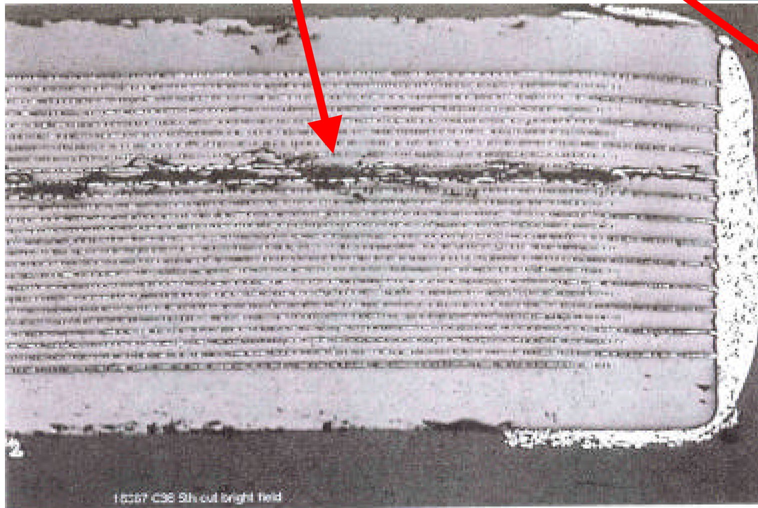
Knit Line Crack (Delamination)

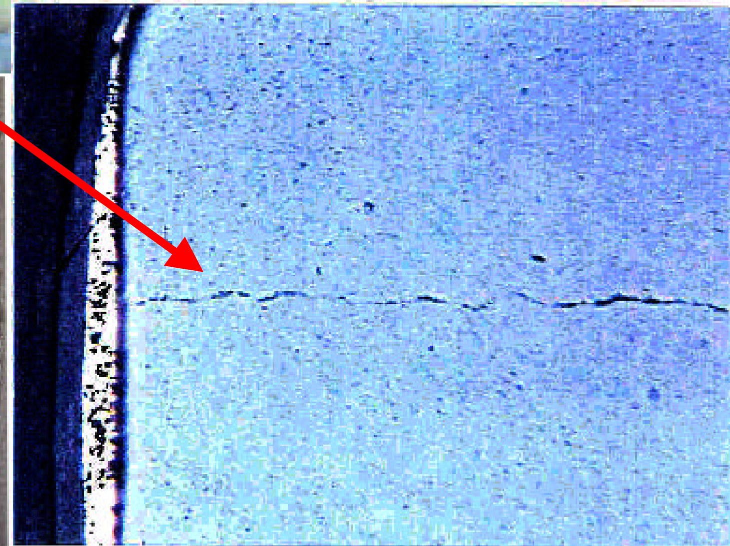


Knit Line Cracks (cont.)

Additional examples

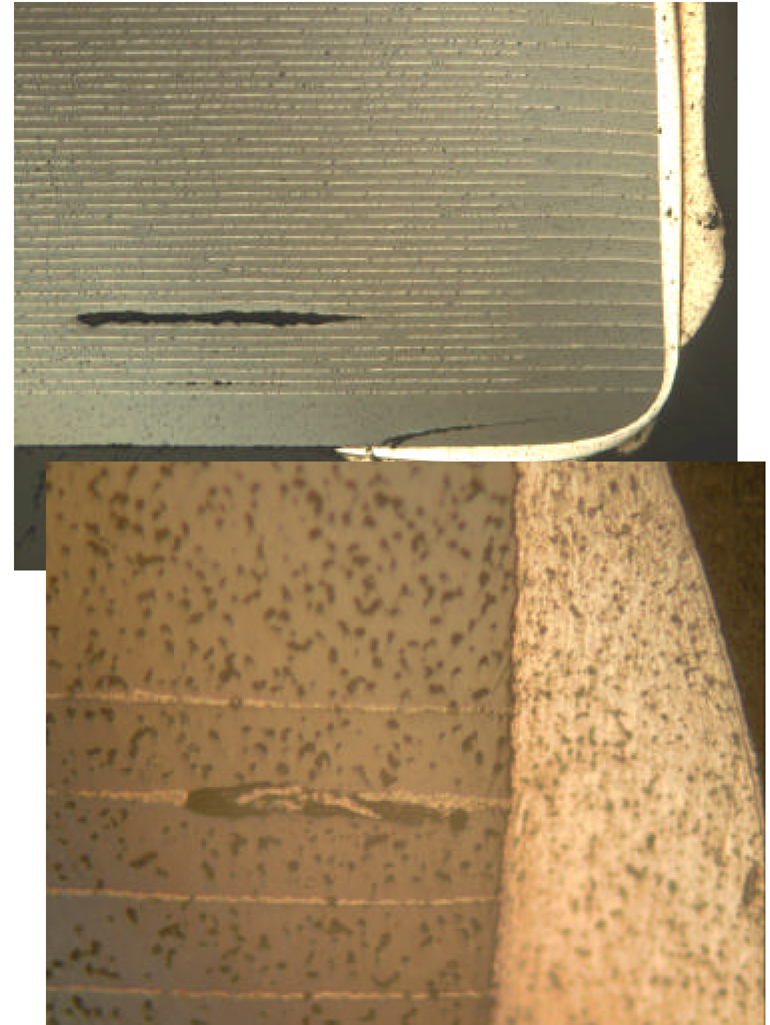






Voiding

- Voids bridging two or more electrodes can become a short leakage current path and a latent electrical defect
- Large voids can also lead to a measurable reduction in capacitance
- Root causes
  - Contamination, both organic and inorganic, in the ceramic powder
  - Non-optimized burnout process

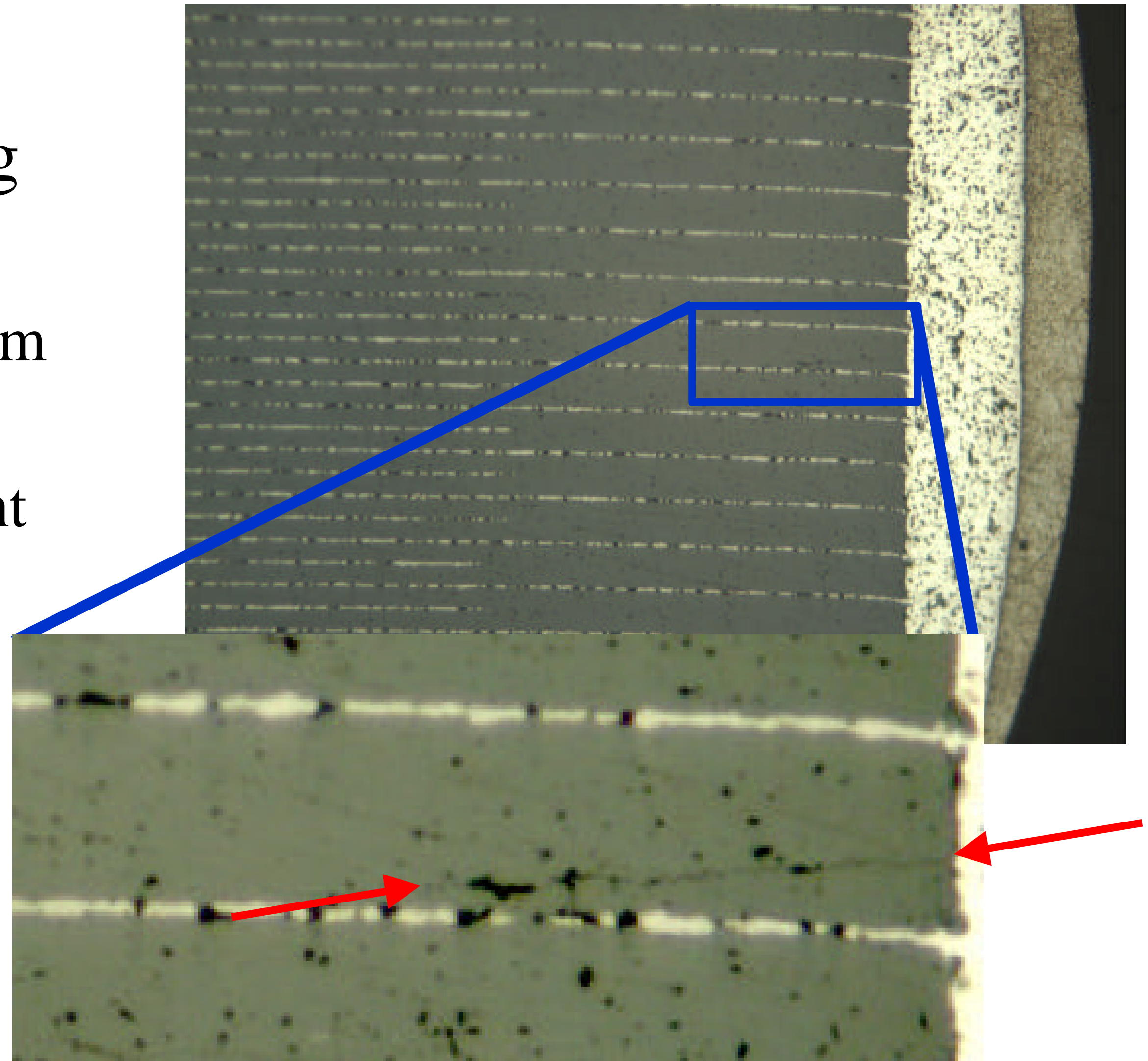


Extrinsic Defects

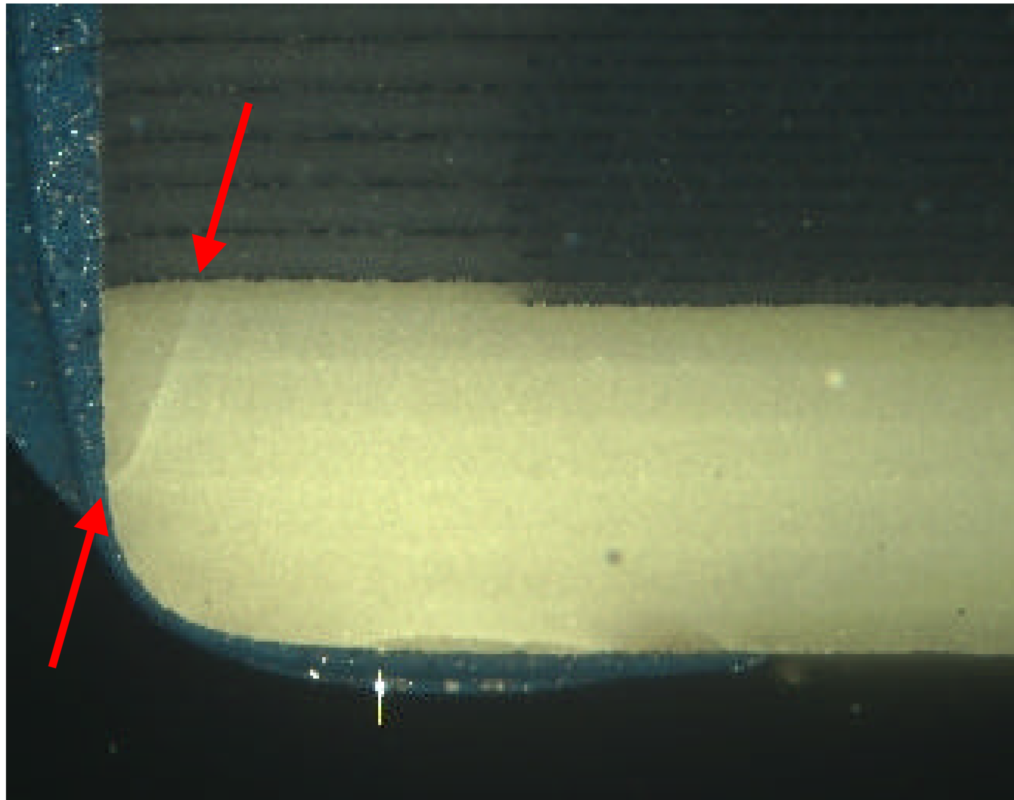
- Extrinsic Defects
  - Handling Cracks
  - Thermal Shock
  - Flex Cracks
  - Silver Migration
  - Tombstoning

Handling Cracks

- Occur during component handling and placement
  - Excessive stress from centering jaws
  - Excessive placement stresses



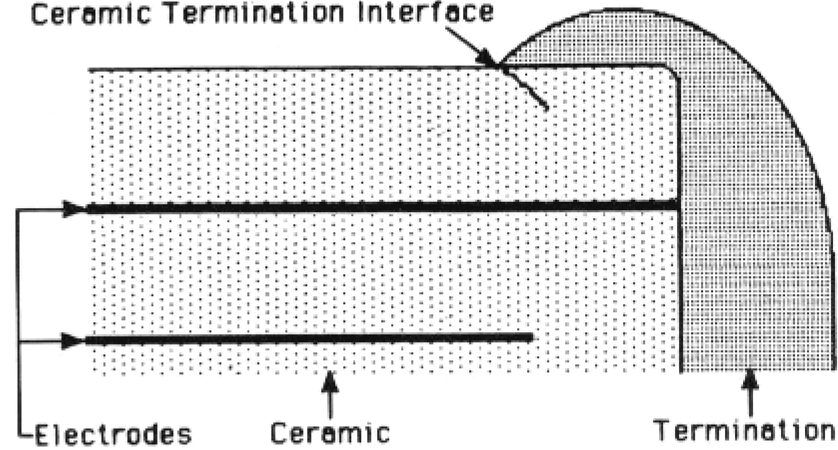
Handling Cracks (cont.)

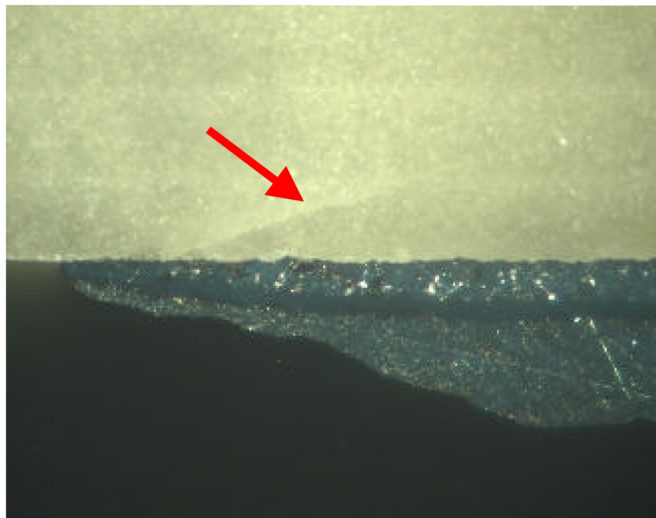


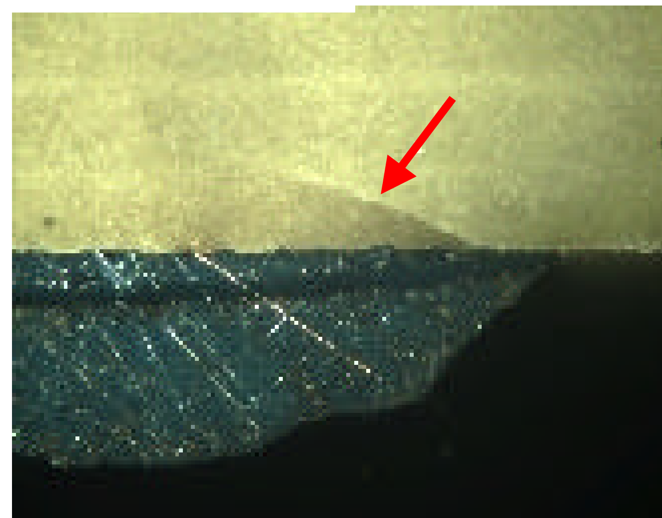
Thermal Shock Cracks

- Occurs due to excessive change in temperature during wave solder, solder reflow, cleaning or rework
- Three manifestations
  - Visually detectable (rare)
  - Electrically detectable
  - Microcrack (worst-case)

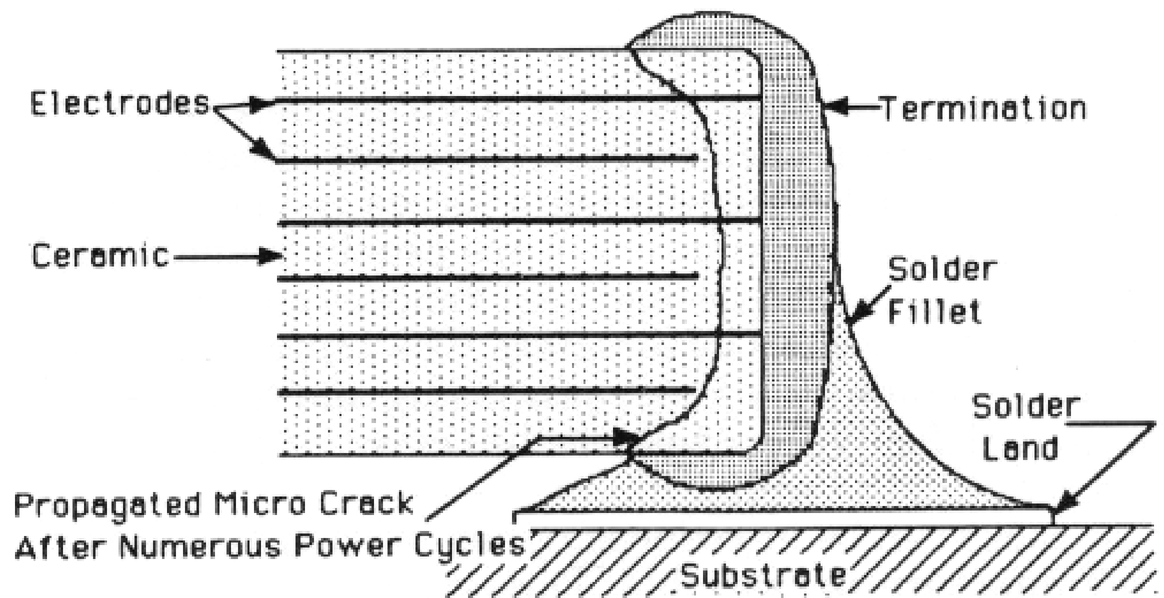
Thermal Shock (microcrack)

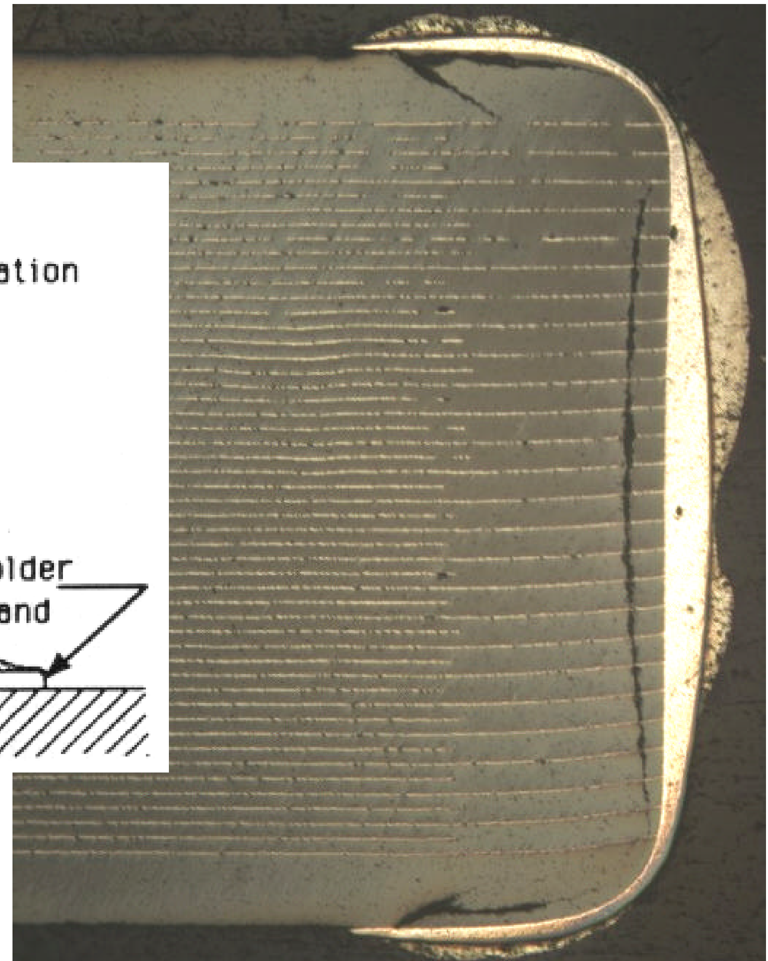






Microcrack (cont.)





Thermal Shock Solutions

- If possible, avoid wave soldering
  - Highest heat transfer rate and the largest temperature changes.
- Minimize rapid temperature changes
  - Room temperature to preheat (max. 2-3°C/sec.)
  - Preheat to approximately 150°C
  - Preheat to maximum temperature (max. 4-5°C/sec.)
  - Cooling (max. 2-3°C/sec.).
- Make sure assembly is less than 60°C before cleaning

Optimum Reflow/Wave Profiles

- Infrared Reflow (IR)
  - Peak temperature of 215-219°C
  - 45-60 seconds above melting point
  - Pre-heat zone at 100° and at 150°C to activate the flux and to allow uniform heating of the board respectively
- Forced Air Convection
  - Better heating efficiency, less sensitive to material properties than IR
  - Temperature gradient across the board becomes much less significant
  - Long soak time not as important
- Wave Solder
  - Belt speeds of 1.2 to 1.5 meters/minute
  - Wave temperature should be 232° ± 2°C
  - Preheat of ~140°C with a dwell time not to exceed 10 seconds

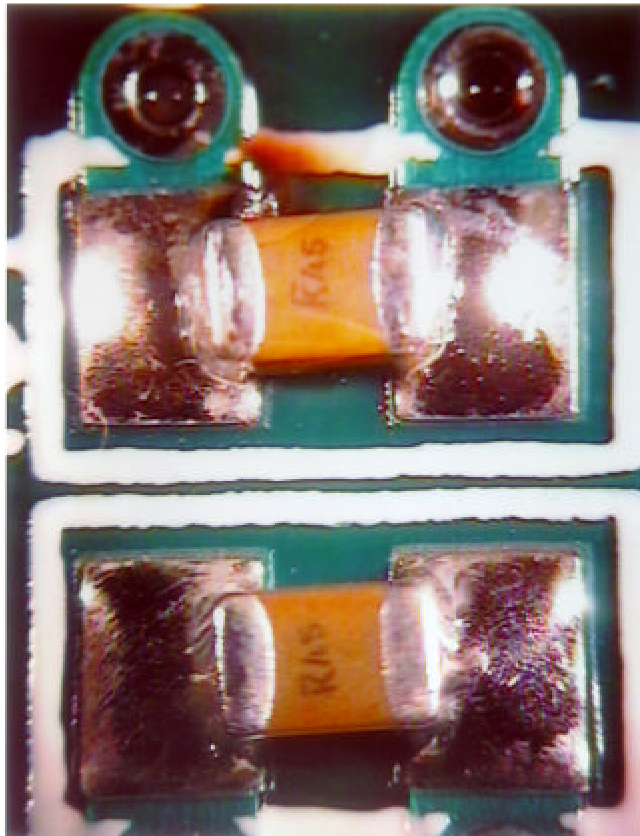
Thermal Shock Solutions

- Use best practices of rework on MLCC's
  - Preheat to 150°C
  - Hot air vs. Solder iron
- Change the capacitor
  - Thinner capacitors
  - Smaller capacitors
  - Choose a dielectric material with a higher fracture toughness (C0G, NP0 > X7R > Z5U, Y5V)
- Change the board
  - Smaller bond pads (reduced thermal transfer)
  - Smaller solder joint fillets

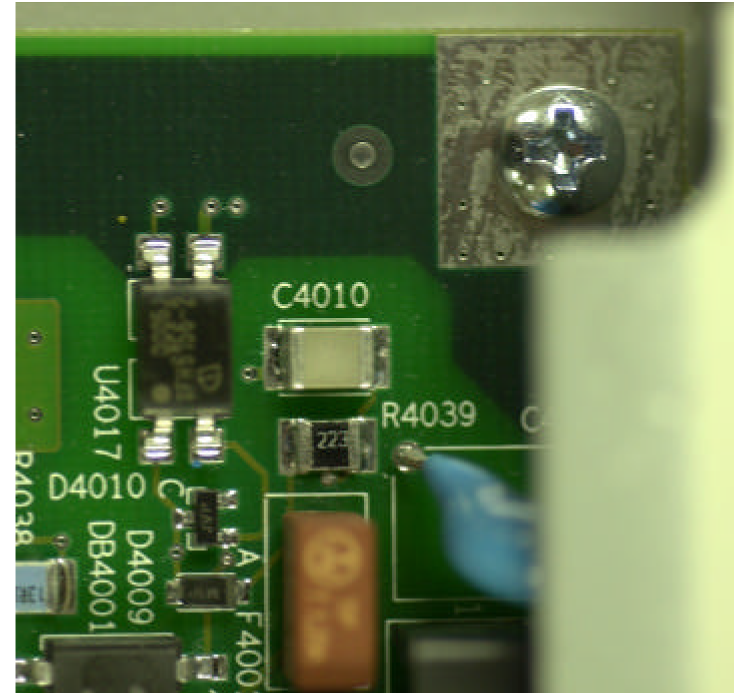
Flex Cracks

- Due to excessive flexing of the board
- Occurrence
  - Depaneling
  - Handling (i.e., placement into a test jig)
  - Insertion (i.e., mounting insertion-mount connectors or daughter cards)
  - Attachment of board to other structures (plates, covers, heatsinks, etc.)

Flex Cracks

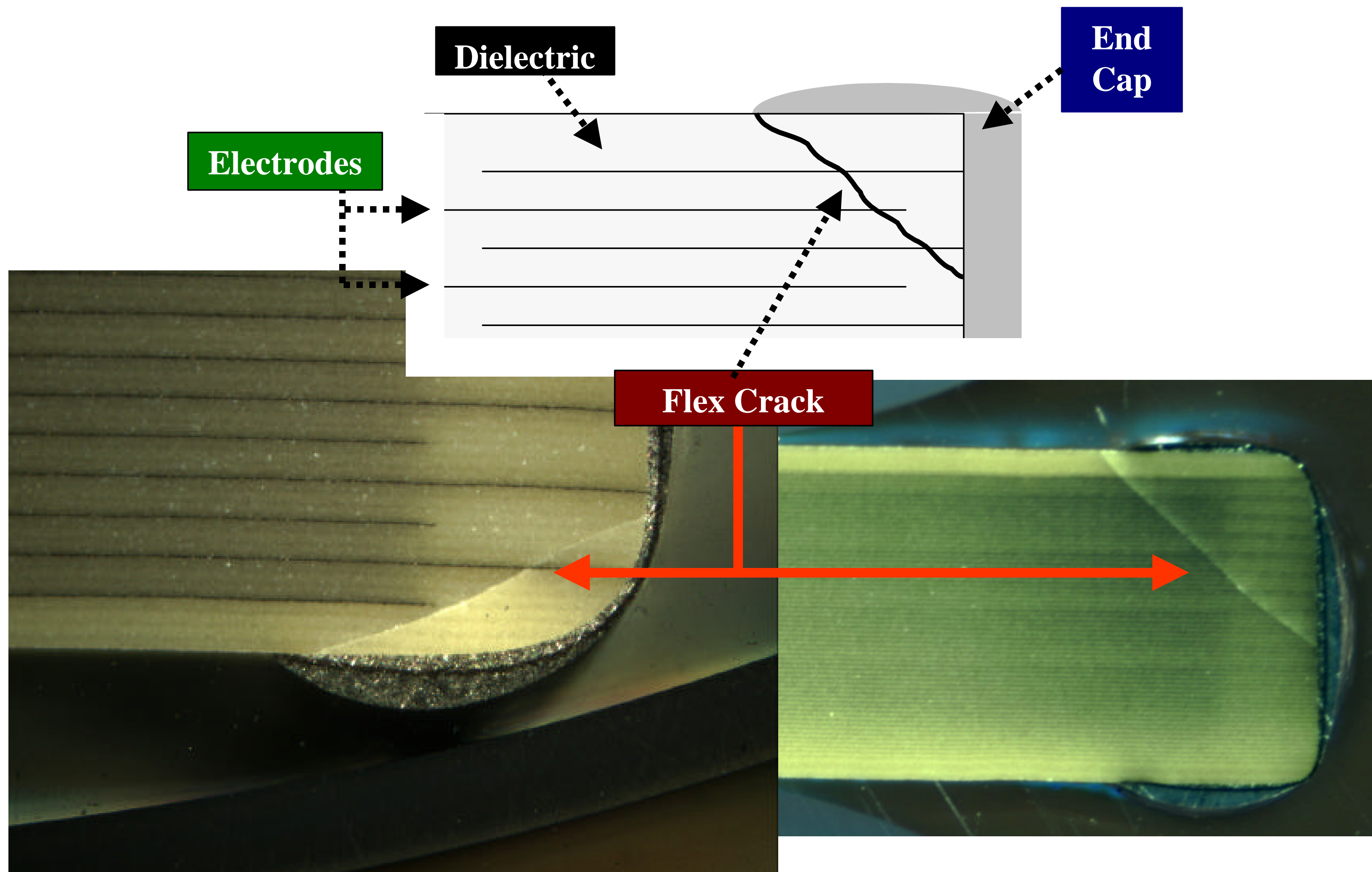


Root Cause:
Connector Insertion

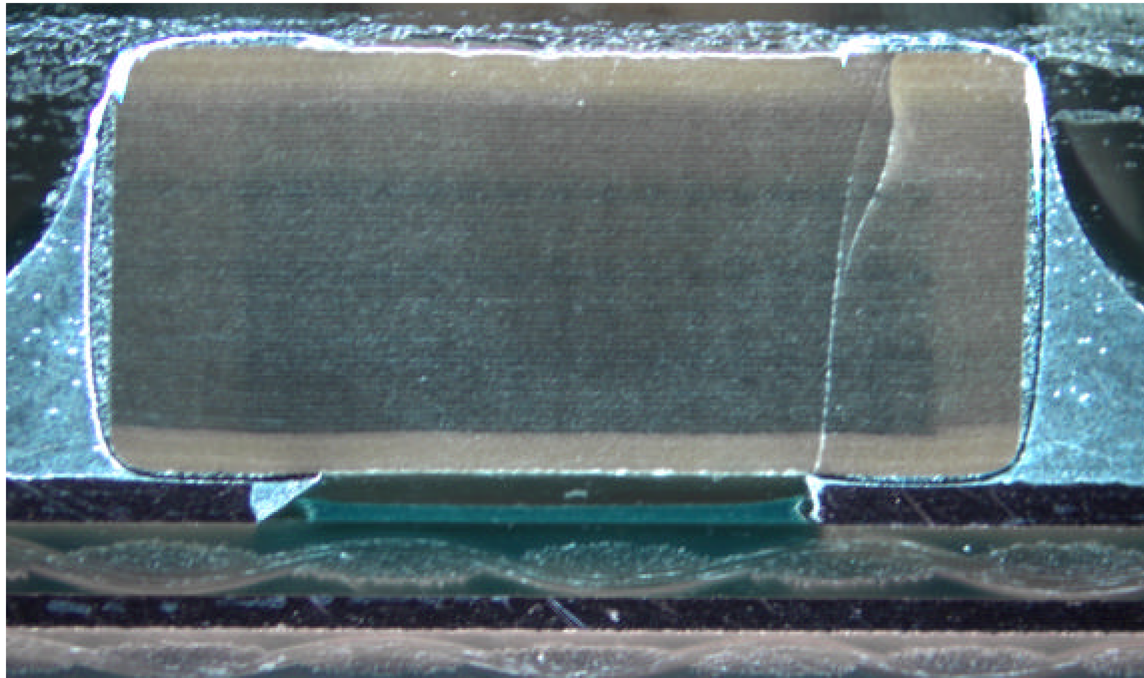


Root Cause:
Tightening of Screw

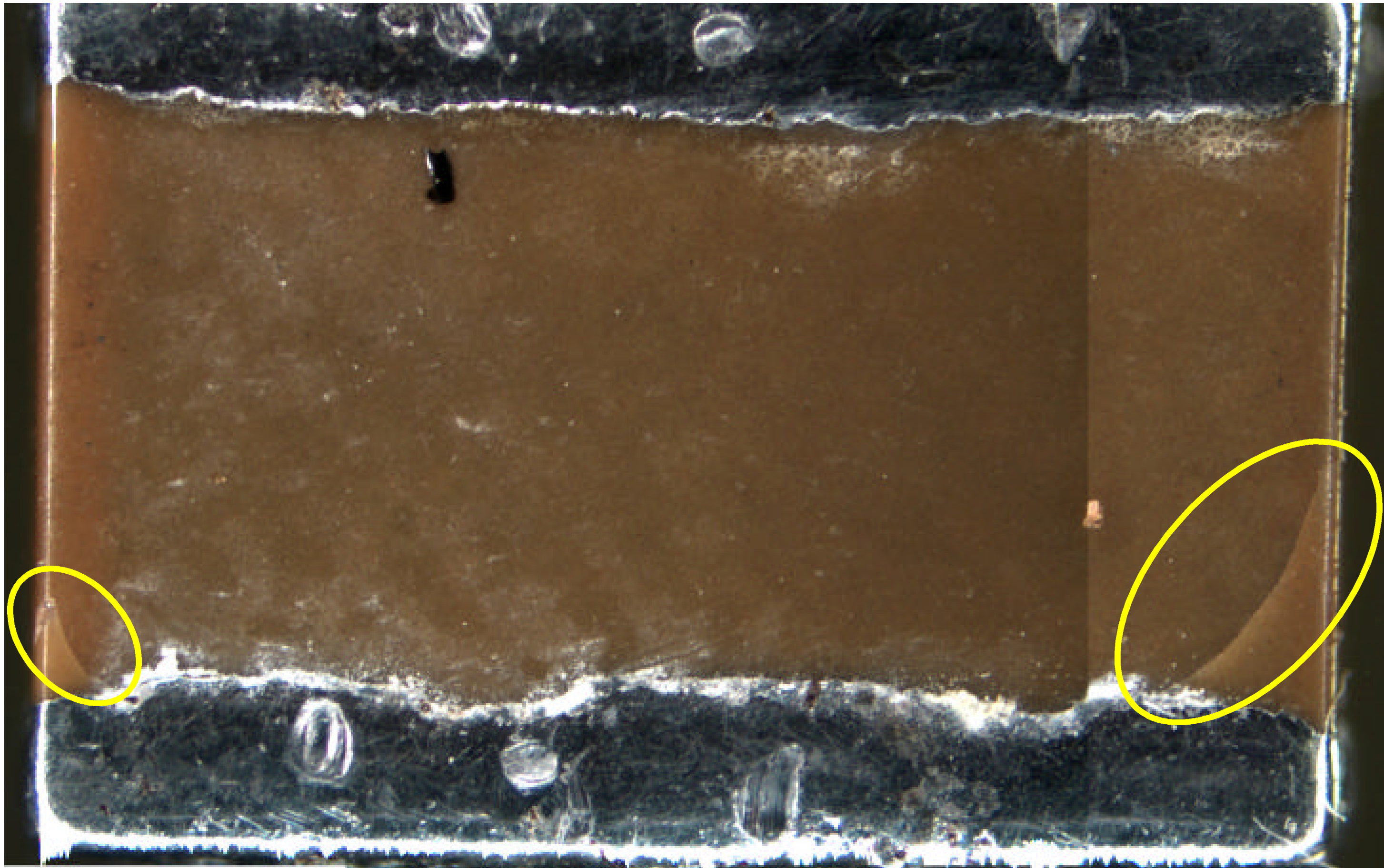
Flex Crack (examples)



Flex Cracks (extreme)



Flex Crack (examples – cont.)

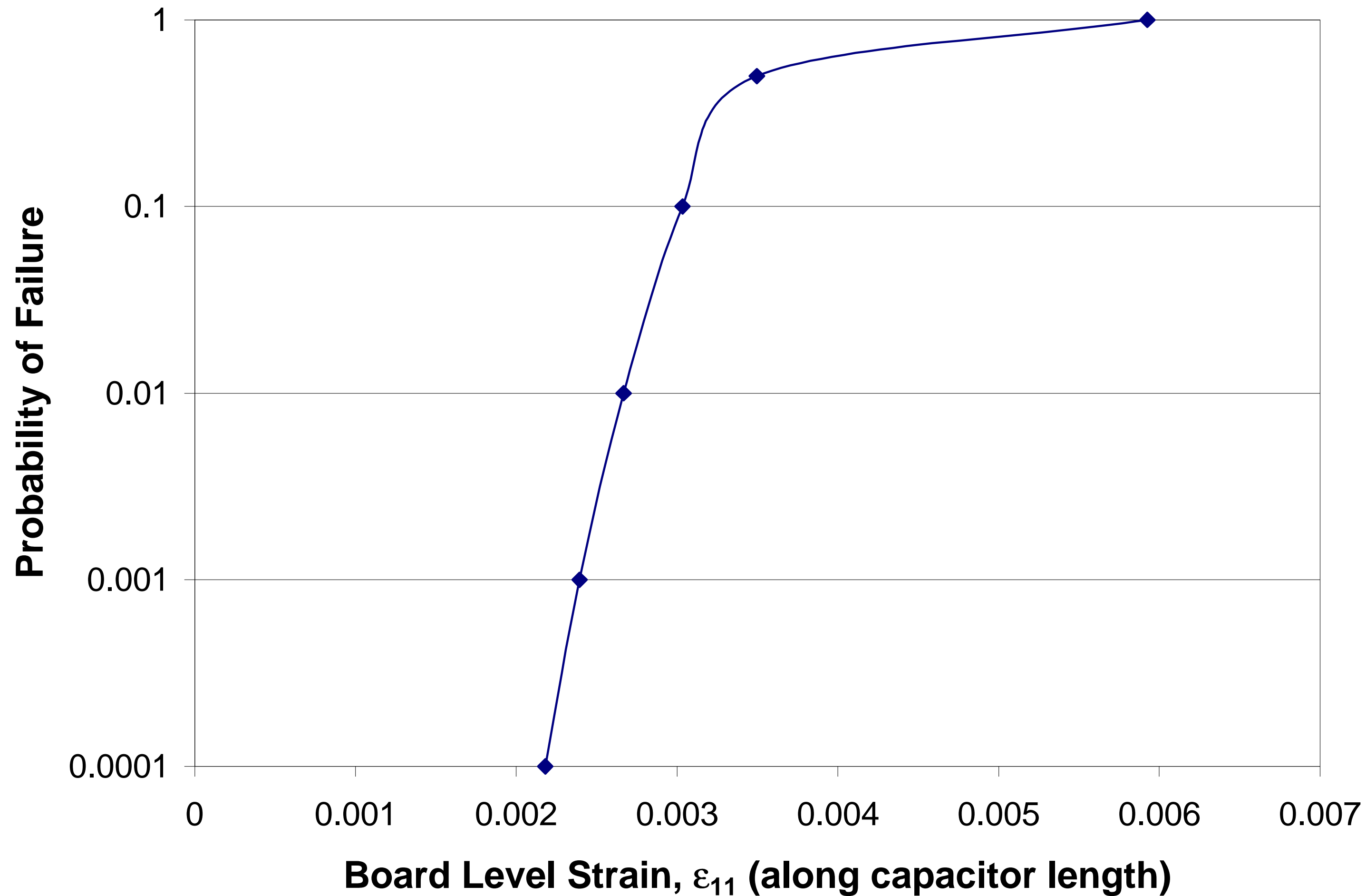


When does Flex Cracking Occur?

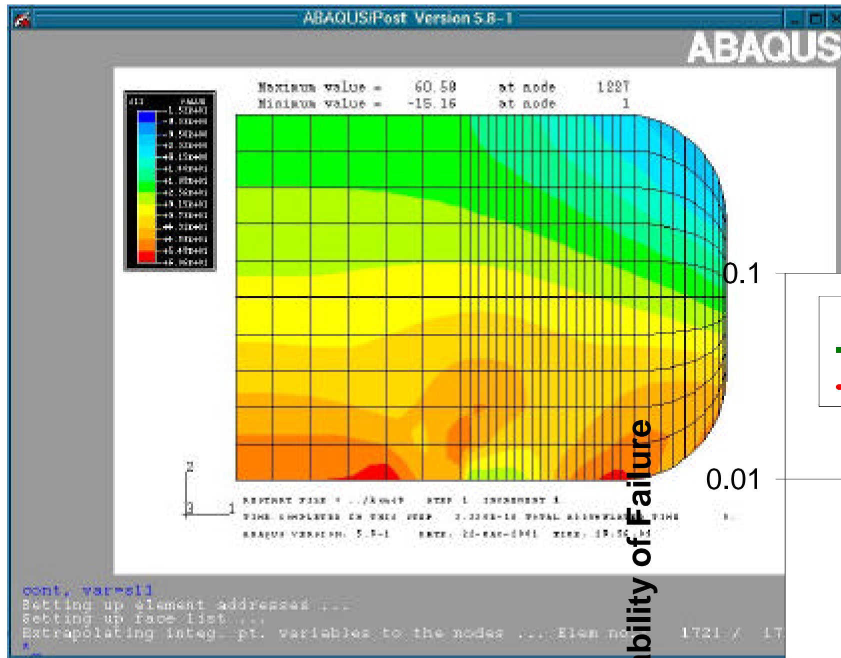
Failure Rate	100ppm	0.1%	1%	10%	50%
Displacement (mm/in.)	1.84 / 0.07	2.02 / 0.08	2.25 / 0.09	2.56 / 0.10	2.95 / 0.12
Radius of Curvature (mm/in.)	367 / 14.4	334 / 13.4	300 / 11.8	264 / 10.4	229 / 9.0
Board-Level Strain	2.18E-03	2.39E-03	2.67E-03	3.03E-03	3.50E-03

Based on bend test performed by Kemet

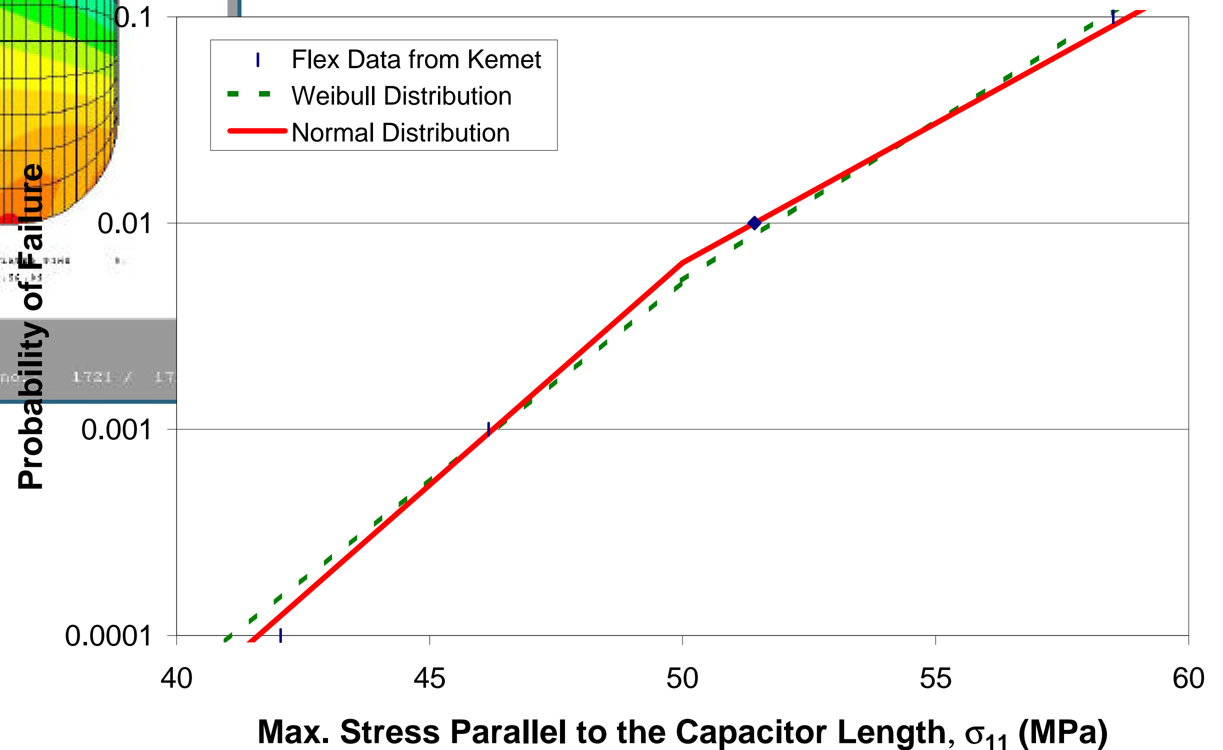
Flex Cracking (board strain)



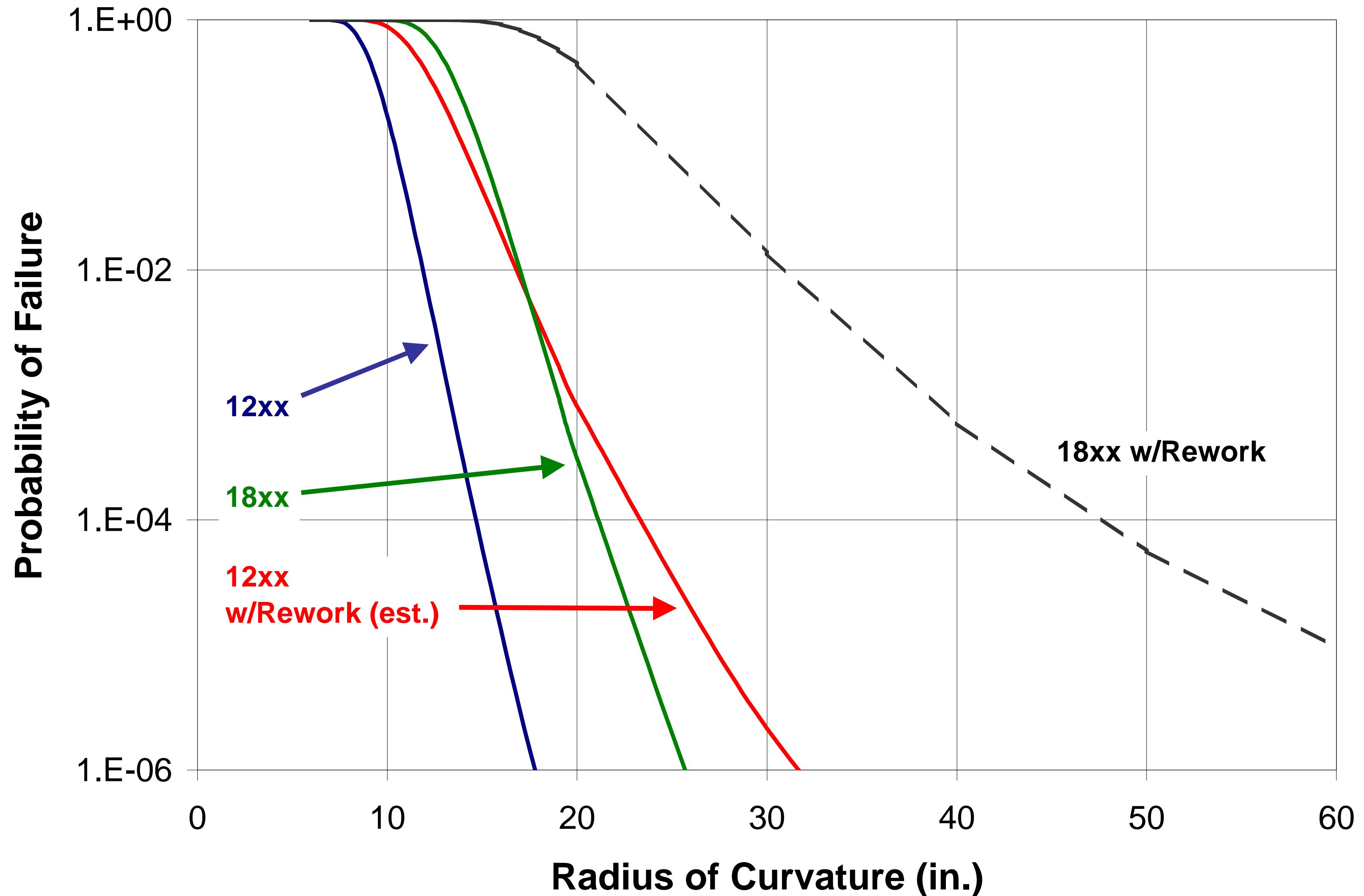
Flex Cracking (internal stress)



CALCE used FEA to determine the internal stress that induces flex cracking



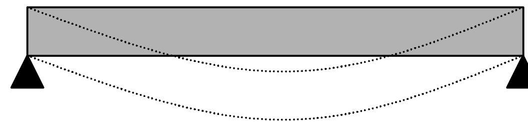
Probability of Flex Cracking



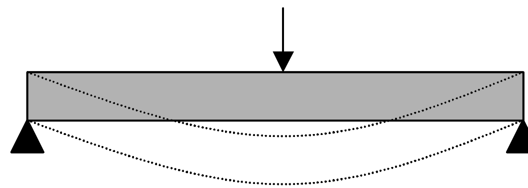
Bend Radius Calculations

<u>Note:</u> Bend radius will be strongly dependent upon attachment configuration.

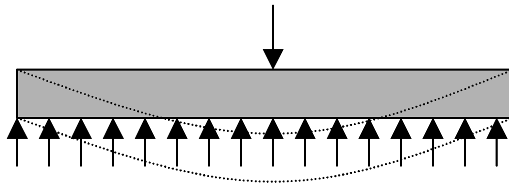
The same displacement can result in 1/3rd the bend radius.



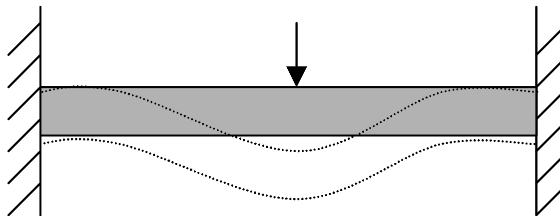
$$\Delta_{max} = L^2/8\boldsymbol{r}$$



$$\Delta_{max} = L^2/12\boldsymbol{r}$$



$$\Delta_{max} = L^2/16\boldsymbol{r}$$



$$\Delta_{max} = L^2/24\boldsymbol{r}$$

Flex Crack Solutions

- Design Changes
  - Smaller capacitors
  - Choose a dielectric material with a higher fracture toughness
  - Reduce bond pad width
  - Replace with tantalum capacitors
  - Improve insertion and bolt tolerances
  - Avoid placing MLCC's near board edges and holes

Flex Crack Solutions

- Process Changes
  - Minimize board warpage
  - Use of board stiffeners
  - Avoid high stress depaneling methods, such as manual break, shear or "pizza cutter". Routing is preferred.
  - Use of torque limiters
  - Appropriate fixturing of in-circuit testing (ICT)
  - Additional training

Silver Migration

- Low standoff height of MLCC's can result in high halide ion concentration
  - Causes migration of the silver-glass frit
  - Can lead to excessive current leakage
- Can be resistant to cleaning

Tombstoning

- Also known as drawbridge
- Root Causes
  - Excessive solder
  - Solder Mask Overthickness
  - Orientation

Screening Strategies

- Primarily dependent upon the defect type
- Avoid if possible (low return on investment)
  - Uses scarce resources (time, money, manpower)
  - Push down the supply chain
- Select non-destructive over destructive

Purpose of Screening

- To prevent failures
- Capacitors store a high amount of energy
  - Charring of the MLCC
  - Damage to adjacent components
  - Destruction of the board or product
  - Damage to customer site

Screening (Intrinsic Defects)

- Visual
  - Low success rate (most defects are internal)
- Xray
  - Very low success rate
- Scanning Acoustic Microscopy (SAM)
  - Includes variants, such as scanning laser acoustic microscopy (SLAM)
  - Very successful on voids and delamination (less so on cracks propagating at 45° or greater)
  - Can be performed internally or through contract work
    - Sonoscan has analyzed over 1 million chip capacitors
    - $65K capital + several days of training

Electrical Screens (Intrinsic)

- Functional Test
  - Medium success rate
  - Most intrinsic defects, except for gross defects have not initiated failure mechanisms, such as increased current leakage or reduced capacitance
- Overvoltage
  - Two modes: High voltage and ionization voltage
    - High voltage (2x rated voltage)
    - 15 volts corresponds to the ionization potential of nitrogen (14.5 eV)
- Piezoelectric testing
  - Recently demonstrated (not widely adopted)
  - Effective on voids and delamination
  - Requires specialized equipment ($??) and training

Environmental Screens (Intrinsic)

- High Temperature Operating Life (HTOL)
  - "Dry" silver migration occurs at temperatures > 120°C
  - Migration behavior well known
- Temperature/Humidity/Bias (THB)
  - "Wet" silver migration will not occur below 65%RH
  - Kemet recommends 24 hours at 85°C/85%RH at 50 volt bias
  - Other research (Hing and Jackson, 1989) suggests a more thorough screen might be 35 hours at 85°C/ 85%RH at 100 volt bias (assumes a 25 micron electrode spacing)
- Both screens are destructive

Screens (Extrinsic)

- Acoustic microscopy is not recommended for extrinsic defects
  - Cracks propagate at 45° or greater
  - Shadowed by the end cap
- Functional test has a medium success rate
- Environmental screens can be very effective
- Methanol soak
  - Methanol is an electrically conductive liquid.
  - Capillary action and low viscosity allow methanol to wick up any surface cracks
  - Conductive film between adjacent electrodes (increase in current leakage)

Summary

- Ceramic chip capacitors can fail
  - Choose a quality supplier
  - If necessary, choose high reliability MLCC's
  - Optimize and control your assembly process
  - Always identify the root-cause of failure

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