Current and CONDUCTORS

The answers to all the age-old questions of current carrying capacity in vias, thermals, planes and traces fall into one simple category: power dissipation. by MICHAEL JOUPPI

Ed: For the sake of space, this article is synopsized. See the complete article and graphs at pcdandm.com.

Electrical traces in circuit boards are sized based on temperature rise as a function of current and conductor cross-sectional area. Belief that temperature rise based on cross-sectional area and current alone is a thing of the past and present, but not the future.

Conductor sizing based on temperature rise, current and cross-sectional area is a starting point. The important piece of information, which has not been available to many designers, is the understanding of what the charts represent. Using charts that dictate the size of traces with no attention given to the joule heating that occurs due to current flowing through the conductors is limiting and causes confusion. A better process is needed.

In 1955, the National Bureau of Standards (NBS) was commissioned to define a set of design guidelines for sizing electrical traces in circuit boards. They found their results had many variables that required further investigation; for that reason they produced a tentative guideline. (They were not funded to continue.) The military adopted this chart, in MIL-STD-275, and later, so did IPC (for IPC-D-275). Lost was the understanding of what the charts represent and how to work with them.

The NBS testing was performed only on external traces. (It was 1955; no one built internal traces.) It was performed with single- and double-sided phenolic and epoxy boards of different thickness. Some had copper planes on the backside; some did not. All these conditions are variables that contribute to the temperature rise of a trace when current is applied. This means that the charts represent an average with respect to the variables in the test samples. From where did the internal trace chart come? The current from the external trace chart was halved.

TABLE 1. Historical Copper Thickness

WEIGHT (oz.)	THICKNESS 1955 (in)	THICKNESS ~1991 (µm – in)	THICKNESS ~2003 (in)
0.5	0.00067	18 - 0.00071	0.0007
1	0.00135	35 - 0.00138	0.0014
2	0.0027	70 - 0.00276	0.0028
3	0.004	108 - 0.00425	0.00425

Conflicting levels of understanding have spread over the years because users consider the chart results as absolute. Absolute, in this context, meaning that a 10°C rise will occur in a trace, when a specific current is applied. This is true for a specific board configuration, suspended in air, for a single isolated trace. But we have not been trained to understand the chart nor have we been given the flexibility to exceed it.

Several problems exist with the charts in IPC-2221 (which replaced IPC-D-275): terminology; lack of an explanation of what the charts actually represent; the data used to develop the external chart are a mix of variables that have an impact on trace temperature; the internal chart is not based on test data.

Copper thickness is not considered as a variable in existing charts. The copper thickness defined in the charts has fluctuated over the years. What should the designer use and how important is the thickness? When one looks at how the charts have changed over time, the differences look like rounding (**TABLE 1**). Look further and one finds the minimum allowable copper thickness, also listed in IPC-2221. The internal copper thickness and the external copper thickness are considerably different than the values being used to determine the width of a trace when the board designed. **TABLE 2** compares the copper thickness specified in the most recent conductor sizing chart and the minimum allowed. Manufactured product can be significantly different than what we designed, of course. This could cause significant problems with respect to internal conductors if a complete understanding of current carrying capacity is not understood.

Copper of 0.5, 1, 2 and 3 oz. are lumped into a single chart. This is fine for low currents (0.5 and 1 oz.), but for 2 oz. and greater copper weights a difference shows up in current carrying capacity. The charts use cross-sectional area as a distinguishing characteristic when sizing traces. As the copper thickness increases there is less current carrying capability for the same cross sec-

tional area. In addition, the charts stop at 3 oz. copper, so a guideline is needed for working with heavier or thicker copper layers.

Let's look at some of the fallacies that have propagated with the charts. Then we will look at variables affecting temperature rise of a conductor as a function of current.

IPC-2221 states, "The temperature rise of a conductor is defined as the temperature (above ambient) as a function of current." It also states that the curves include a nominal 10% derating (on a current basis) to compensate for normal variations in etching techniques, copper thickness, conductor width estimates and cross-sectional area. Additional derating of 15% is suggested when the panel thickness is 0.8 mm or less and the conductor thickness is 108 µm or thicker. Notes such as this give the impression that the temperature rise is well understood: in fact, it is not.

The curves do not have a 10% derating and in fact the external trace chart is not conservative for what it actually represents. They are not derated and comments such as this are confusing. The only way to understand the charts is to understand how, where and when the data were collected to them. While 15% derating for panel thickness of 0.8 mm or less is on the right track and can be seen in the original data, one can also see that no derating exists.

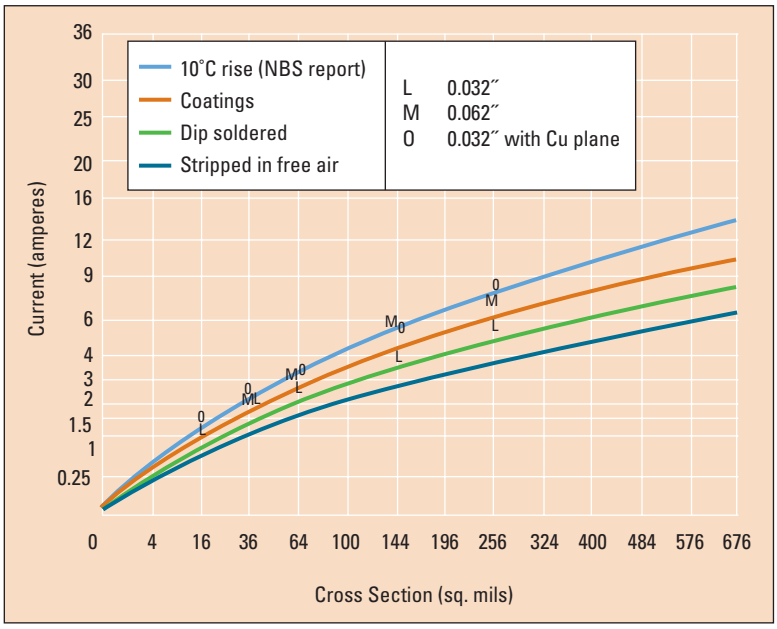

FIGURE 1. The impact of material on thermal conductivity varies substantially because the IPC are the result of estimations, not actual tests.

A review of the original data allows us to evaluate the impact of some of the variables hidden in the existing charts. For example, look at board thickness. L and M, in **FIGURE 1**, are NBS boards from 1955 that are 0.032″- and 0.062″-thick boards, respectively. A 2 Amp difference is seen between these test boards for the same 10°C rise. This difference is due to board thickness. The thinner board has less cross-sectional area to conduct the heat away from the trace. Recent test results and analysis show the same results.

Another variable that influences this chart is the presence of a copper plane. The letter O represents a 0.032″-thick board with a copper plane on back. We can see that the combination of the thin board and copper plane creates a comparable result with the thicker board (M). Recent tests and analysis, not to mention common sense, also show significant effects on trace temperatures due to the presence of copper planes.

There are several ways that the internal copper in a board can be taken into consideration. One is to investigate the effective thermal conductivity of the board.

The thermal conductivity provides an understanding of the materials capability of spreading heat. There are two ways to look at this board material property. One is to look at the dielectric material itself and another is to investigate the effective thermal conductivity from the composite in which we include the dielectric material and the copper. Copper has three orders of magnitude greater thermal conductivity than the dielectric material. When the copper thermal conductivity is used to calculate the effective thermal conductivity of the composite, a significant difference is noticed vs. the dielectric only. Considering the dielectric only is what the charts are supposed to represent.

The composite has a significant effect when determining the steady state temperature rise. If we do not take into account the copper planes in a design and we only consider the board material itself we see delta T's as shown in **FIGURE 2** for an internal trace. Many find this chart surprising due to the marked difference between the IPC values and the others listed. Reason: The IPC values do not represent test results; they represent half the current from the external trace-sizing chart.

A look at the effective thermal conductivity reveals the impact of copper on heat spreading capability. **FIGURE 3** compares test results from a polyimide board with model results in which the thermal conductivity of the board uses the effective thermal conductivity. The PolyCuLyrs category represents a 0.07″-thick, nine-layer board with four power/ground layers with 70% copper coverage, four signal layers with 20% and one at 5% copper coverage. The polyimide category represents a test board with test traces only and no copper planes.

TABLE 2. Allowable Copper Thickness (Industry Standard)

	ALLOWABLE CHART				
	% Diff	µm	In.	µm	In.
Internal					
0.5 oz.	-48.2	12	0.00047	17.8	0.0007
1 oz.	-42.2	25	0.00098	35.6	0.0014
2 oz.	-27.0	56	0.00221	71.1	0.0028
3 oz.	-18.6	91	0.00358	108.0	0.00425
External					
0.5 oz.	46.1	33	0.00123	17.8	0.0007
1 oz.	25.5	46	0.00181	34.3	0.00135
2 oz.	6.4	76	0.00299	71.1	0.0028
3 oz.	-0.9	107	0.00421	108.0	0.00425

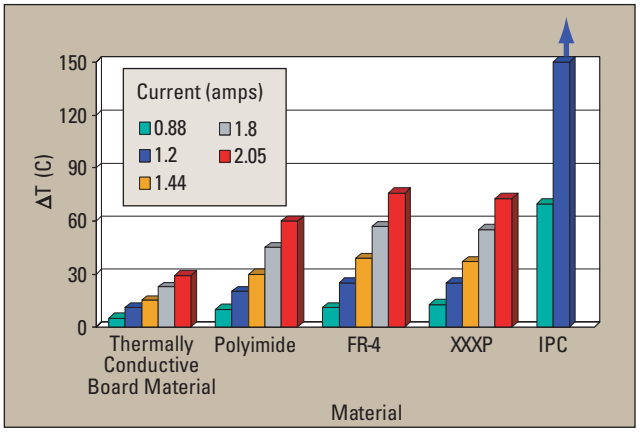

FIGURE 2. Delta T's for one trace, with respect to current, for a thermally conductive laminate, polyimide, FR-4 and XXXP, and the values as determined by IPC-2221.

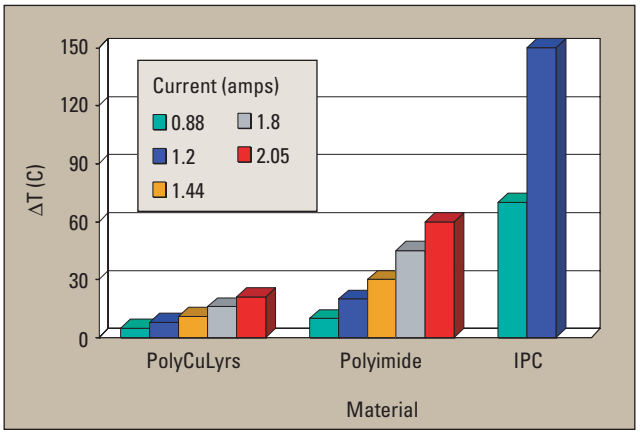

FIGURE 3. The composite thermal conductivity impact shows how conservative the IPC standard is.

It is easy to see why most applications have had few problems over the years: 1) The external charts are non-conservative, but the thickness is greater than what we design; 2) the internal trace thickness is significantly thinner than what we design, but the chart is overly conservative; 3) board thickness is covered in the notes, so compensation is made there; 4) not only are we conservative with both charts, but all the copper in the boards helps even more; 5) they are even more conservative, once mounting configurations and convective environments are accounted for.

The charts are warm and fuzzy. The problem is, warm and fuzzy is hard to quantify. For example, what happens with very thin and small boards, vias and microvias? Or for 200 to 300 Amps?

Studies Underway

Traces, vias, microvias, thermals, embedded resistors, planes, their maximum current capability and design optimization: This is where we are headed.

Vias and thermals can be designed to manage both the amount of current required and provide relief from internal copper, to permit soldering. The only issue is that the optimum thermal resistance of the wagon wheel is in the process of being determined. Initial studies show that a significant amount of current can be applied to small sections of copper that are tied to a plane. There is a study in progress to determine the optimum amount of copper to permit designers a better guideline to size thermals.

Common questions are, what temperature can the traces be, and how hot can they be without damaging the board? The response is, this is not the main issue, unless a design has traces only on the board. Components, their peak temperature and their performance are of primary concern. Typically, a semiconductor device's life will be extended if it operates at a lower junction temperature. From a system perspective, using less energy is desirable. Understanding the issues in the electrical design, mechanical design, manufacturing and assembly and taking into consideration as many of these disciplines as possible are what is needed to make good design decisions. These include component junction temperatures, peak temperatures for capacitors and resistors, solder joints and temperature cycling. Rather than be concerned with the temperature of the trace, look at the heating introduced by traces, planes and vias. When these effects are considered, they can be added to the other heat sources in a design. This leads to the power dissipated in the board by the traces, vias and planes.

This brings us to the first semester of thermodynamics and the conservation of energy, or the first law. Using the first law and considering a circuit board with all its components as a control volume, we can investigate this. Evaluating the energy into the control volume, and the energy out of the control volume, we can look at an energy balance. When we perform this energy balance, something that we have been neglecting for years emerges: the energy into the system from the traces, planes and vias.

Power in traces and vias at first seems to be negligible. The problem with assuming that the power is negligible is that it gets ignored and can become a problem when it is not well understood. Answers to age-old questions of current carrying capacity in vias, thermals, planes and traces fall into one simple category: power dissipation. Being able to manage the power dissipation is what controls temperature rise in a board.

Every design is different: applying a single chart to all applications is not the answer. Design rules that include power density and total board power are a missing link that is being defined. These design rules are the basis of IPC-2152, a standard under development to provide a better understanding of trace sizing. PCD&M

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MIKE JOUPPI just started Thermal Man Inc., and has developed a calculator for sizing traces, vias, thermals, planes and embedded resistors. He has 20 years of experience as a thermal mechanical engineer with Hughes Aircraft, Lockheed Martin and Coretec. He is chairman of the IPC-2152 task group. He can be reached at mikej@thermalman.com.