Designing for EMC

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This paper, which has been around for some years, has been updated at the beginning of 2010 to incorporate some new ideas and edit some old ones.

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Introduction

The main EMC problems for electronic products are the emissions of internally-generated high frequencies which may interfere with on-board or nearby radio reception, and susceptibility to transient or radio frequency interference from the external environment which may degrade the quality of analogue signals, or corrupt digital processes. EMC standards specify levels and test methods for both of these groups of phenomena. A further requirement which comes under the umbrella of the EMC Directive is that the mains supply input current should be limited in its harmonic content.

If they are dealt with as an integral part of the product design, these requirements are not hard to meet. Too often, because they do not affect the visible performance of the product, they are not considered until the design is substantially complete and production is about to start. Incorporating EMC principles as an afterthought is expensive and time-consuming. Only 15% of products which have not been designed for EMC are likely to pass EMC testing first time; on average between one and two re-designs (and re-tests) are necessary before such products are certifiable.

Cable coupling

A major part of the coupling path for interference from the product to the environment and vice versa is through its connecting cables. These form efficient transducers with the outside world, via conduction at low frequencies and via radiation, particularly around their resonant frequencies (at which the cable length is a multiple of a quarter wavelength). Although the cables may intentionally carry high-frequency signals, such as data or video, a more potent interference source is common-mode noise coupled onto the cable at the interface, and flowing in all its conductors or in its screen (Figure 1). This common mode noise may not be directly related to the intended signal. For a digital circuit, it could be due to noise developed in the 0V or power rail network by the operation of other circuits; for instance microprocessor or video clock frequencies could appear on a serial data port. Ethernet clocks at harmonics of 25MHz could appear on the power connector.

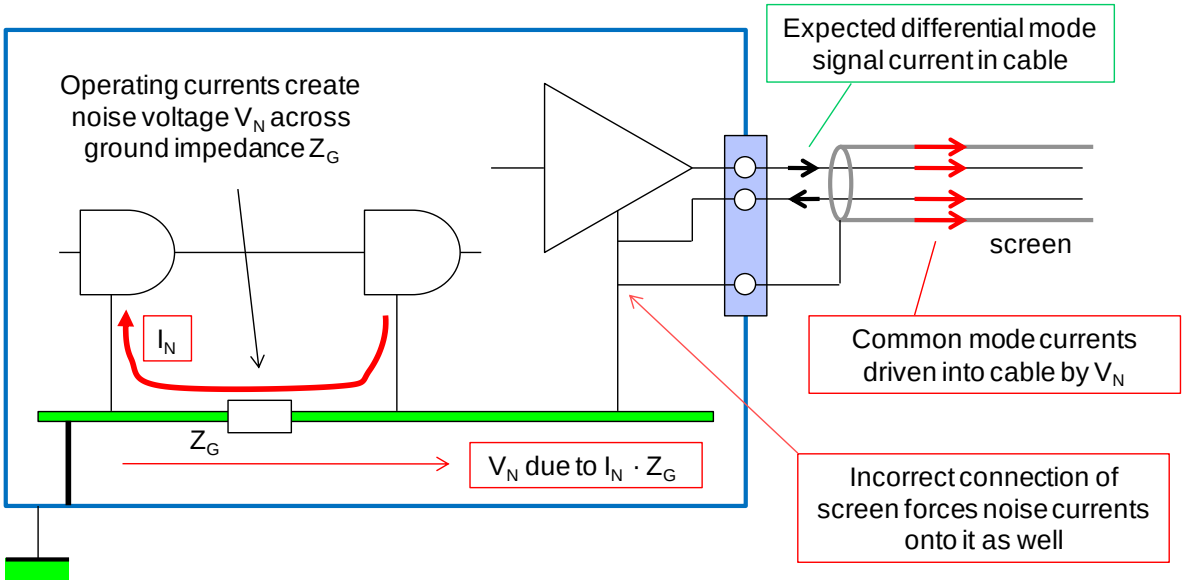

Figure 1. Common mode interface current

A major part of EMC design is therefore concerned with the interfaces between the unit and its cables, which normally means filtering. But if the noise is present on the 0V circuit reference as well, then filtering to this reference will be ineffective. So we have to control the noisiness of the circuit itself, which leads into circuit design and PCB layout. If you have no cable interfaces, you're halfway there already – but only halfway.

Direct coupling

The rest of the way involves controlling the interaction of the product's internal circuits directly with the external environment. This means that all internal structures – particularly PCBs and wiring, but also conductive metal parts such as heatsinks and chassis members – must be designed to minimize their effectiveness as accidental antennas. PCB layout is a topic in itself, but the general principle throughout is that conductive parts should be bonded together to stop HF potentials arising between them.

But this principle has to be applied with some thought. Take the example of a heatsink. Heatsinks can be a particular cause of EMC difficulties on PCBs. The concern is the effect of heatsink stray capacitance on emissions either from digital devices carrying RF voltages, such as microprocessors and ASICs, or from switching power components such as MOSFETs or triacs.

A simplified equivalent circuit of a PCB with a 0V plane, a processor, a heatsink on the processor, and an enclosure around the whole assembly is shown in Figure 2. The processor is the source of the RF noise: voltages V_N on the silicon at clock frequencies appear with respect to the 0V plane and are capacitively coupled directly to the metal of the heatsink. The heatsink must have good thermal contact to the chip, and a by-product of this is a high coupling capacitance C1. In its turn, the heatsink is a large chunk of metal, and it has a high capacitance C2 to its surroundings, particularly the enclosure.

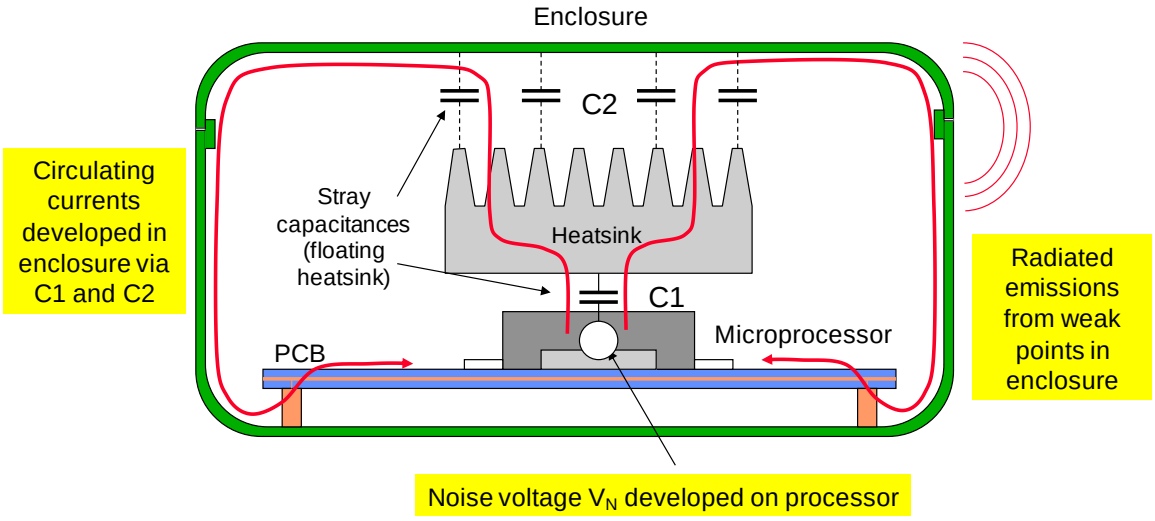

Figure 2. The heatsink coupling problem

This energizes the entire enclosure with circulating currents at the clock frequency and its harmonics. Any weakness in the enclosure will allow these frequencies to radiate. To control this, the most effective measure is to prevent the heatsink from carrying high levels of clock noise. This means it must be referenced to the 0V plane on the PCB, and cannot be allowed to float. Capacitance C1 and noise source V_N cannot be removed, but if the heatsink is referenced to 0V then the circulating noise currents remain in its locality and the voltage on the heatsink is minimized. The enclosure itself is not stressed, since C2 is not fed from a noise source.

To avoid high frequency resonances with the capacitance of the heatsink, the inductance of the 0V connection needs to be well below 1nH to be effective, and this means that multiple 0V contacts around the outside of the heatsink must be provided. The most effective designs use a continuous conductive gasket around the periphery of the heatsink (which must be conductively finished) to a ground plane contact strip on the surface of the PCB.

What this equivalent circuit shows is that the one place *not* to connect the heatsink to, is the enclosure. If this is done, then the capacitance C2 has been bypassed and all the noise coupled through C1 flows in the enclosure, which is bound to worsen emissions. The only cure in this case would be to reduce C1 or incorporate a screen to 0V between the device and its heatsink, each of which introduces difficulties. This example demonstrates the need to consider mechanical conducting structures – the heatsink and the enclosure – as electrical components.

Grounding and PCB layout

The classical definition of a ground is "an equipotential point or plane which serves as a reference for a circuit or system". Unfortunately this definition is meaningless in the presence

of ground current flow. Even where signal currents are negligible, induced ground currents due to environmental magnetic or electric fields will cause shifts in ground potential. An alternative definition for a ground is "a low impedance path by which current can return to its source". This emphasizes current flow and the consequent need for low impedance, and is more appropriate when high frequencies are involved. It is important to remember that two physically separate "ground" points are not at the same potential unless no current is flowing between them.

Careful placement of ground connections goes a long way towards reducing the noise voltages that are developed across ground impedances. But in any non-trivial circuit it is impractical to eliminate circulating ground currents entirely. The other aspect of ground design is to minimize the value of the ground impedance itself.

Ground impedance is dominated by inductance at frequencies higher than a few kHz, and the inductance of a PCB track or wire depends mainly on its length. For example a 10cm length of 0.5mm track appears as 60nH while a 2cm length is 12nH. Paralleling ground tracks to form the ground layout in a grid structure maximizes the number of different paths that ground return current can take and therefore minimizes the ground inductance for any given signal route. The limiting case of a gridded ground is when an infinite number of parallel paths are provided and the ground conductor is continuous, and it is then known as a ground plane. This is easy to realize at the PCB level on a multilayer board and offers the lowest possible ground path inductance, provided that it is not interrupted by other tracks. Note that the purpose of the ground plane is not to provide shielding but to give a low high-frequency ground impedance.

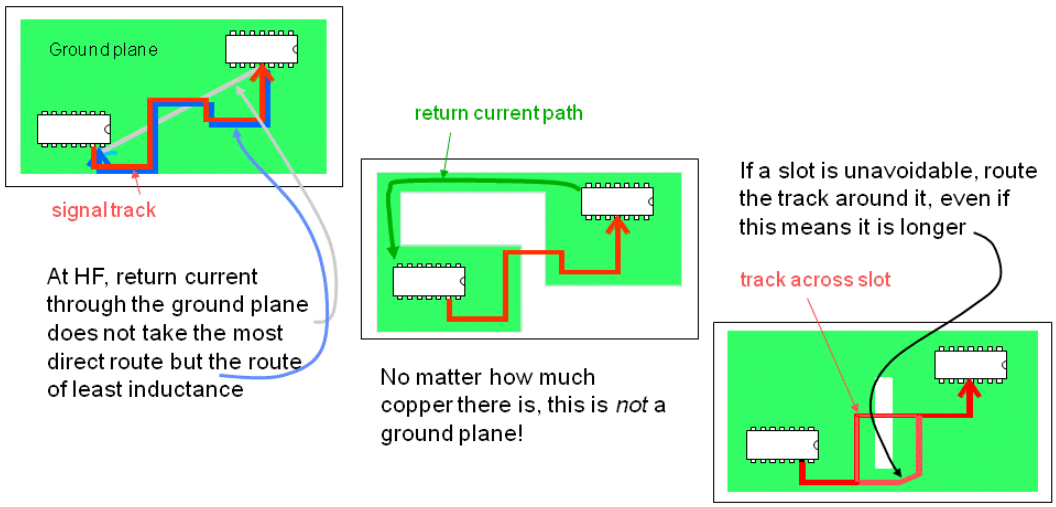

Figure 3. Breaks in the ground plane

The first important rule is that there should be no breaks in the plane layer underneath critical tracks (emissive or susceptible nodes), which would divert return current flow and hence increase the effective loop area (Figure 3); nor should these tracks be located near the edge of the plane. Thus it is necessary before starting the layout to identify which these critical tracks are. The criteria include ranking them in order of frequency and di/dt (for emissions) and in

order of bandwidth, impedance and level (for analogue immunity) or whether or not they are latched (for digital immunity). Reset inputs are always critical.

The second important rule is that any such critical tracks should be routed as close as possible to the ground plane layer, i.e. on the next adjacent layer in multilayer boards. The thinner the layer spacing, the more effective is the ground plane. Power supply rails (tracks or planes) can be as critical as signal tracks, since they carry significant levels of clock energy. Even when they are decoupled, the higher frequencies of the clock harmonics benefit from the attenuation provided by a high inter-layer capacitance.

The effect of reducing the ground inductance within the circuit is to minimize self-generated ground noise in digital circuits (V_N in Figure 1), and to minimize the differential ground voltages generated by incoming interference. But these cannot be entirely eliminated, and therefore the interface grounds must be laid out so that interference currents are diverted harmlessly away from the circuit (incoming) and from the cables (outgoing).

One approach to ground plane design is to use a single 0V plane for all the circuitry on the board, which avoids the difficult and messy process of deciding exactly where to split the planes. But this doesn't prevent interface currents from passing into or out of the circuit 0V. Another is to create a separate interface ground reference. The I/O cables (including the mains) should be grouped together and the ground for the filtering and shielding of these cables should be taken to the metal case at this point, if it is present.

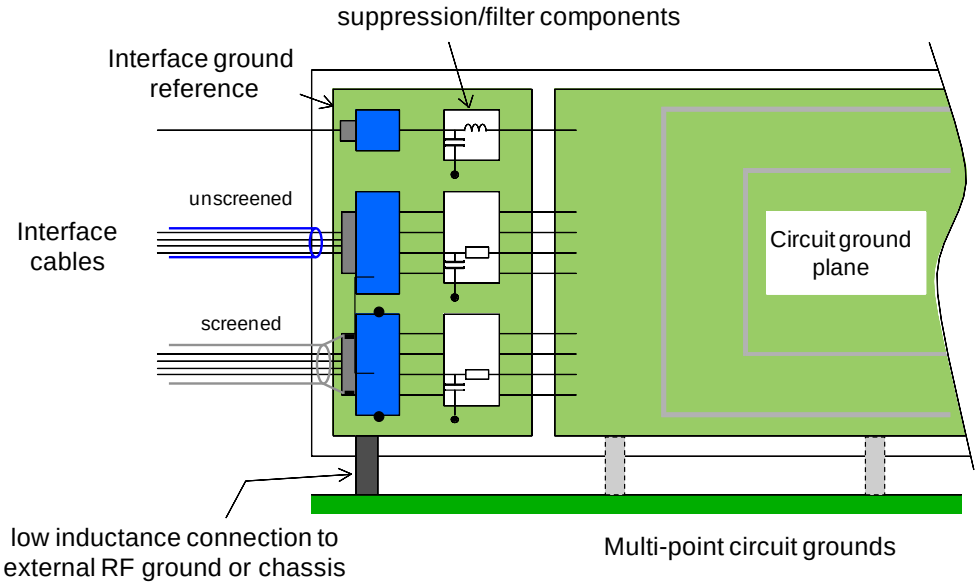

Figure 4. The interface ground reference

Dealing with common-mode interference currents at the interfaces is essential. This is achieved by creating a low transfer impedance ground structure to which all interface lines are decoupled at RF. Its purpose is to minimize RF and transient potential differences across the ports. It can be realized very simply either by using a metal or metallic plate on which to mount all the connectors, or by designating a part of the PCB as an interface ground reference

plane for the same purpose (Figure 4). It implies that all connector interfaces are located in the same area of the product, and this is definitely the best approach. If connectors *must* be mounted at opposite ends of a circuit board, then the interface ground structure must span the whole length of the board, from one connector to the other. This is easiest with a separate metal chassis plate on which the PCB is mounted.

This interface ground reference should always be an integral part of the design even though it does not appear on a functional circuit diagram. It does not need to have either a circuit connection or an external ground connection for EMC purposes, though either may be wanted for circuit or safety reasons. Any cable shields should not be taken to the PCB 0V but directly to the interface ground reference via the shortest route.

Filtering

Unshielded I/O lines should be decoupled to the interface ground reference at the point at which they enter or leave the enclosure (Figure 4). The purpose of this is to bypass interference currents so that they do not flow into the circuits or out through the cables. RF filter capacitors and chokes are necessary for this. Capacitors must be mounted with short leads and close to the ground to which they are decoupling to minimize their stray inductance, and chokes should be wound and mounted to minimize capacitance across the winding. Suppression ferrite chips are useful for reducing common-mode cable currents at high frequencies.

For interference purposes, treat the mains port just like any other, especially as regards decoupling it (with Y-rated capacitors) to the interface ground reference. A mains filter is essential if you are using a switch-mode power supply. Even if not, mains transient immunity is markedly improved if a filter is included (provided that other interfaces are also treated properly). The attenuation performance of mains filters is very much tied in with their size. If you are space- or weight-limited, you will need to put a lot more effort into designing the power supply for low emissions and high immunity before the filter is considered. Both common- and differential-mode paths must be looked at; transformer and heatsink design play a crucial part, as do the choice of switching components such as MOSFETs and diodes to minimize high frequency generation.

It is most important to ensure that the filter has good high frequency performance and is properly installed. The earth connection of the filter unit must make good low-impedance contact to the interface ground reference and even a short length of wire can have a degrading effect on the filter performance. Assured metal-to-metal contact is highly desirable.

If you know that the equipment will be used in an environment subject to high-energy surges, or if its compliance requirements include the surge test, then varistor-type surge limiters will be necessary on the mains port (unless the voltage parameters of the power supply components are heavily over-rated).

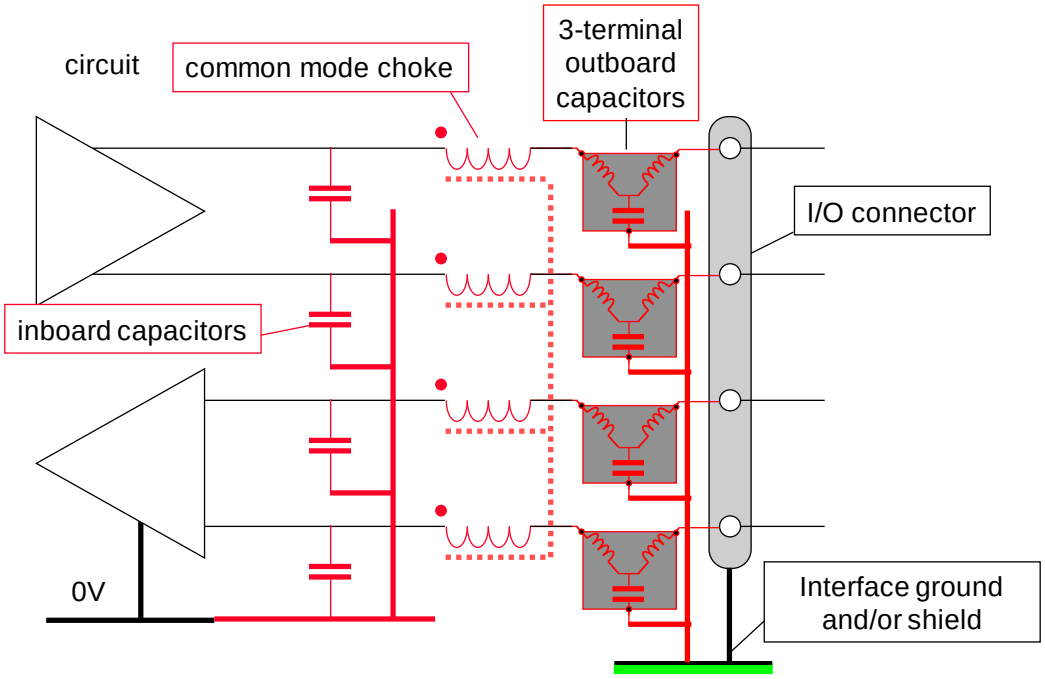

Figure 5. Interface filtering

There are two ways to circumvent the problem of common-mode currents on signal cables: screen them or filter them (Figure 5). Either technique presupposes the existence of the interface ground, and one or other is essential. If using screened cables, determine what transfer impedance is necessary for the cable screen, and make sure that you specify cables of adequate performance. Crucially, the cable performance is irrelevant if the screening is degraded by a poor quality connection to the interface ground. If at all possible, avoid pigtails and make sure complete screen coverage is maintained through the connector shells to the reference point. If pigtails are unavoidable, make them short, and don't bother to specify an expensive cable.

If the interface can be filtered, a screened cable may be unnecessary. All lines in the interface must be filtered, including 0V lines. Filters can consist of parallel (preferably 3-terminal) capacitors directly to the interface ground, series common-mode wound or ferrite chokes, or a combination of both. The configuration will depend on the common-mode impedance on each side of the interface, for which an educated guess is usually necessary - but remember that a consensus exists (expressed, for example, in IEC 61000-4-6) that the average RF common-mode impedance of a cable is 150 ohms. The advantage of series chokes is that on their own they need no ground connection, which can be helpful for wideband circuits (and is of course essential if the design has omitted the interface ground reference), though this is offset by their relatively poor performance when used alone.

Control analogue signal bandwidths

Filtering at the circuit level: many analogue circuits have no difficulty with emissions and need have no difficulty with immunity, provided that their operating bandwidth is properly controlled. Both modulated RF and electrical fast transient bursts can have a disastrous effect

on untreated analogue circuits if the layout, filtering and screening techniques are only partially effective. Circuit techniques include (Figure 6)

- tailoring feedback networks for the minimum necessary bandwidth, while making sure that this doesn't affect stability;
- including in-line RC low pass filters, especially at inputs;
- adding ferrite beads or resistors in series with the input pins of high gain circuits such as op-amps and comparators; likewise adding low-value (e.g. 47pF) capacitors directly across such inputs, if this can be done without compromising stability.

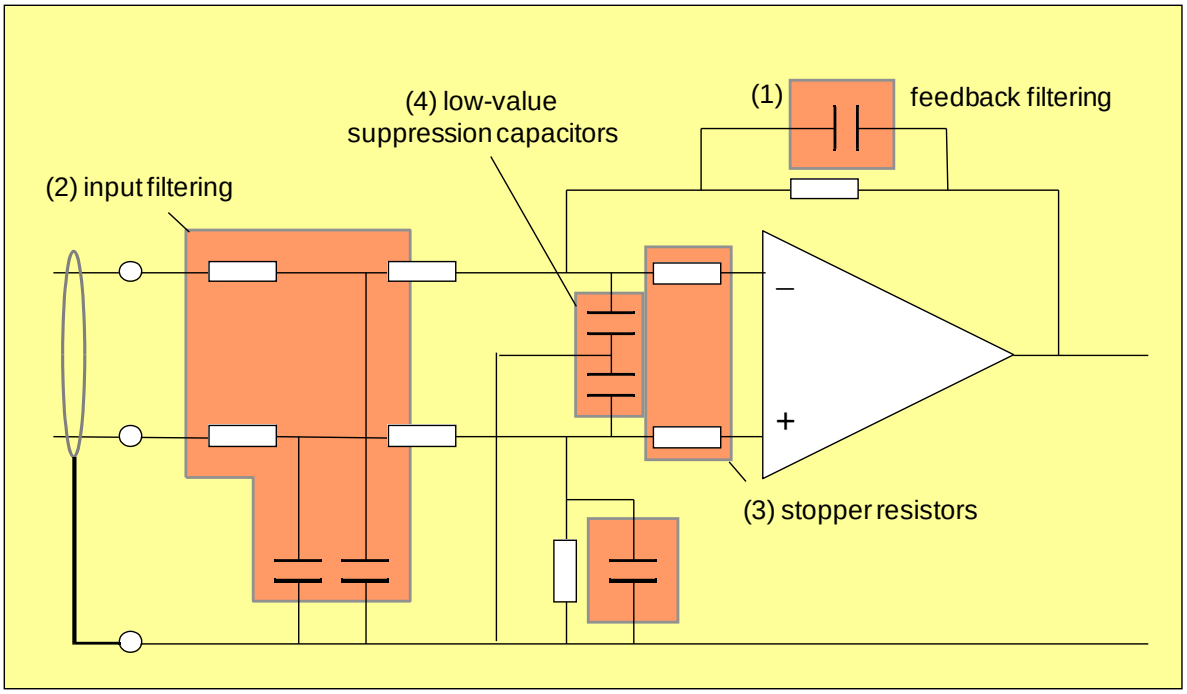

Figure 6. Circuit bandwidth limiting

Use a conductive enclosure

Or, put the unit in a screened box. For very noisy or very susceptible circuits this may be a necessary part of the overall strategy, but it is ineffective unless all the other approaches are also followed. Interfaces form a breach in the screening and must be filtered or screened as above. Viewing and ventilation apertures and other discontinuities where there is no assured electrical contact between parts, such as seams and doors, also form a breach and must be treated if the screen is not to be degraded; but for only moderate (e.g. 20dB) low frequency screening effectiveness they can be tolerated. At these levels of screening the material used for the enclosure is of little importance, and conductively coated plastics can give perfectly adequate performance. It is still quite possible with good PCB layout practice and proper interface control, to meet the requirements of the less onerous commercial standards without a screened enclosure at all.

Very often the greatest merit of a conductive enclosure is not as a screen but as a low-transfer-impedance grounding structure. In this case provided that discontinuities are outlawed in those parts of the structure where a low ground impedance is essential, they can be acceptable elsewhere. The interface ground reference referred to above is then an integral part of the enclosure structure; cable screens are bonded to it, as are interface filter capacitors and mains filters.

Shielding effectiveness is determined largely by the ratio of the wavelength of the highest frequency of interest to the dimension of apertures or seams in the shield, so these dimensions should be minimized. A reasonable target to aim for is that no hole or slot should exceed one-tenth of a wavelength (3cm at 1GHz) in its longest direction. To improve screening performance, mating seams between panels in the case should be fitted with conductive gaskets or spring fingers to ensure a conductive path across the seam. Ventilation holes or louvres are acceptable provided that they are constructed from several small holes or slots rather than one large one. As should be obvious, the worst screening degradation occurs next to such apertures, so noisy or sensitive components shouldn't be located near them.

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