Chapter

# 3

# EMI Filter Design

Nearly all power circuits contain an input electromagnetic interference (EMI) filter. The main purpose of the EMI filter is to limit the interference that is conducted or radiated from the power circuit. Excessive conducted or radiated interference can cause erratic behavior in other systems that are in close proximity of, or that share an input source with, the power circuit. If this interference affects the power circuit, it can cause erratic operation, excessive ripple, or degraded regulation, which can lead to system level problems. Input EMI filters may also be used to limit inrush current, reduce conducted susceptibility, and suppress spikes. The specifications for the allowable interference are generally driven by the power circuit specification. The most common specifications include MIL-STD-461 for military applications and FCC for commercial applications. Many other EMI specifications also exist.

This chapter will deal with the design and analysis of EMI filters that will reduce conducted interference and conducted susceptibility and limit inrush current. The design of the input filter is slightly more critical when the power circuit is a regulated switching circuit, rather than a linear circuit, because a negative input resistance is created by the regulated switching circuit.

Although it is possible to simulate the radiated interference of a power circuit, it is beyond the scope of this book.

## Basic Requirements

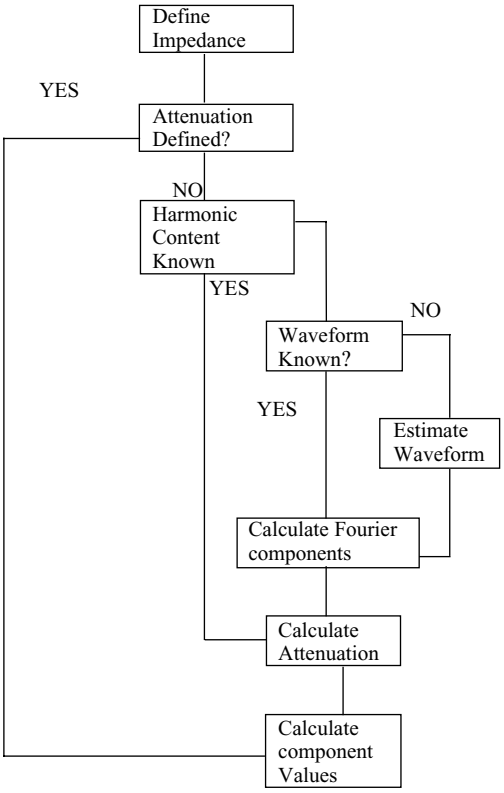
The design of an input EMI filter begins with the definition of two basic requirements:

- The filter must provide the power converter with lower output impedance than the negative input resistance of the power circuit.

- The input filter attenuation must be sufficient to limit the resulting interference to a level that is below the imposed specification.

The following flowchart provides a step-by-step approach that may be used to design an input filter.

**EMI filter design flowchart**




## Defining the Negative Resistance

The negative resistance of the power circuit can be defined by looking at the following conditions

$$P_{\text{in}} = \frac{P_{\text{out}}}{\text{efficiency}}$$

$$I_{\text{in}} = \frac{P_{\text{in}}}{V_{\text{in}}}$$

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{V_{\text{in}}^2}{P_{\text{in}}} = \frac{V_{\text{in}}^2 * \text{efficiency}}{P_{\text{out}}}$$

The input resistance is negative because as the input voltage increases, the input current decreases. As a simple example, we can use PSpice to analyze the input resistance of the power circuit. PSpice can analyze the input resistance in a number of ways. The simplest method is the transfer function (.TF) analysis, which calculates the DC gain and the small signal input and output impedance. The following example uses the PSpice.TF analysis to measure the input resistance of a switching power circuit.

**Example 1—Input resistance analysis**

**Input File**

```
RIN: INPUT RESISTANCE
.TF V(5) V1
V1 5 0 20
G1 5 0 Value = { 100/V(5) }
.END
```

**Output File**

```
RIN: INPUT RESISTANCE
.TF V(5) V1
V1 5 0 20
G1 5 0 Value = { 100/V(5) }
.END

.END

***SMALL-SIGNAL CHARACTERISTICS

V(5)/V1 = 1.000E+00

INPUT RESISTANCE AT V1 = −4.004E+00

OUTPUT RESISTANCE AT V(5) = 0.000E+00
```

The G1 source simulates a power circuit, which has an input power of 100 W. V1 applies 20 VDC to the power circuit, and the .TF measures the input impedance at node 5 and the output impedance at V1. The results are placed in the output file. Note that PSpice calculated the input impedance as a negative resistance of 4 Ω, which is in agreement with the above derivation.

## Defining the Harmonic Content

The next step in designing an input EMI filter is to determine the harmonic content of the power circuit input current. If the input current waveform is known, a Fourier analysis can be performed in order to establish the harmonic content of the waveform; however, even if the exact waveform is not known, we can estimate the waveform with reasonable accuracy. The design can be optimized later, if necessary.

Consider the pulsating waveform in Fig. 3.1. With a peak amplitude of 1 and a base amplitude of 0, we can compute the Fourier series of

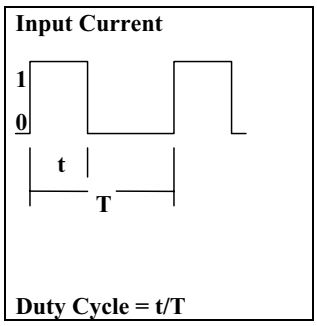



**Figure 3.1** Pulsating waveform used in the Fourier series computation.

harmonic $n$ as follows:

$$A_n = \frac{2}{T}\int_0^t \sin(nt)$$

$$B_n = \frac{2}{T}\int_0^t \cos(nt)$$

$$C_n = \sqrt{A_n^2 + B_n^2}$$

If we assume that the input ripple current is pulsating and if we know the duty cycle, we can proceed to the Fourier analysis. If the duty cycle is not known, we will assume a value of 50%. This assumption is the worst case, because the Fourier analysis of a pulsed waveform has a maxima at a value of 50%. In the next example, we will use SPICE to calculate the Fourier coefficients of a 50% duty cycle pulse.

### Example 2—.FOUR analysis

The following example demonstrates the use of the .FOUR analysis. V1 is a pulsed voltage source, which has a 50% duty cycle and a 100-kHz frequency. The .FOUR statement calculates the magnitude and phase of the DC value and the first nine harmonics. The result is placed in the output file as shown below.

```
EX2: DEMONSTRATING THE USE OF THE .FOUR ANALYSIS
.OPTIONS NUMDGT=3
.TRAN .01U 20U
.FOUR 100KHZ V(1)
V1 1 0 PULSE 0 1 0 0 0 5U 10U
.END
```

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(1)

DC COMPONENT = 5.010000E-01

| HARMONIC NO | FREQUENCY (Hz) | FOURIER COMPONENT | NORMALIZED COMPONENT | PHASE (DEG) | NORMALIZED PHASE(DEG) |
|---|---|---|---|---|---|
| 1 | 1.000E+05 | 6.366E-01 | 1.000E+00 | -3.600E-01 | 0.000E+00 |
| 2 | 2.000E+05 | 2.000E-03 | 3.142E-03 | 8.928E+01 | 9.000E+01 |
| 3 | 3.000E+05 | 2.122E-01 | 3.333E-01 | -1.080E+00 | 4.088E-09 |
| 4 | 4.000E+05 | 2.000E-03 | 3.142E-03 | 8.856E+01 | 9.000E+01 |
| 5 | 5.000E+05 | 1.273E-01 | 2.000E-01 | -1.800E+00 | 2.044E-08 |
| 6 | 6.000E+05 | 2.000E-03 | 3.142E-03 | 8.784E+01 | 9.000E+01 |
| 7 | 7.000E+05 | 9.093E-02 | 1.428E-01 | -2.520E+00 | 5.723E-08 |
| 8 | 8.000E+05 | 2.000E-03 | 3.142E-03 | 8.712E+01 | 9.000E+01 |
| 9 | 9.000E+05 | 7.072E-02 | 1.111E-01 | -3.240E+00 | 1.226E-07 |

TOTAL HARMONIC DISTORTION = 4.288115E+01 PERCENT

As you can see from the output file, the fundamental harmonic has a peak value that is 63.6% of the peak pulse amplitude. Although this does provide the required information, it is far from elegant. A better solution is to calculate the harmonics in Probe. The resulting plot is shown in Fig. 3.2.

This is the worst case for a pulsed waveform and could be conservatively used for the design of the input filter.

### Example 3—Using the .STEP command to calculate harmonics

The next example uses the PSpice .STEP command to sweep the duty cycle from 5% to 95% and look at the fundamental amplitude of the resulting square wave. As in the previous example, V1 is a pulsed

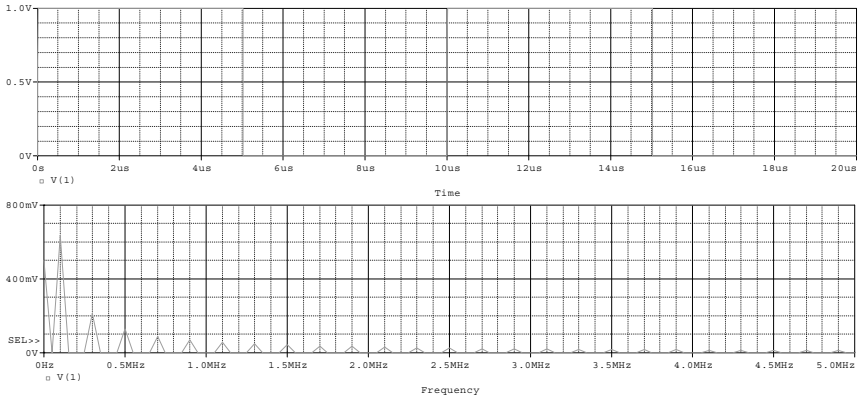



**Figure 3.2** The FFT feature of the Probe graphical waveform postprocessor is used to calculate the harmonics of a square waveform.

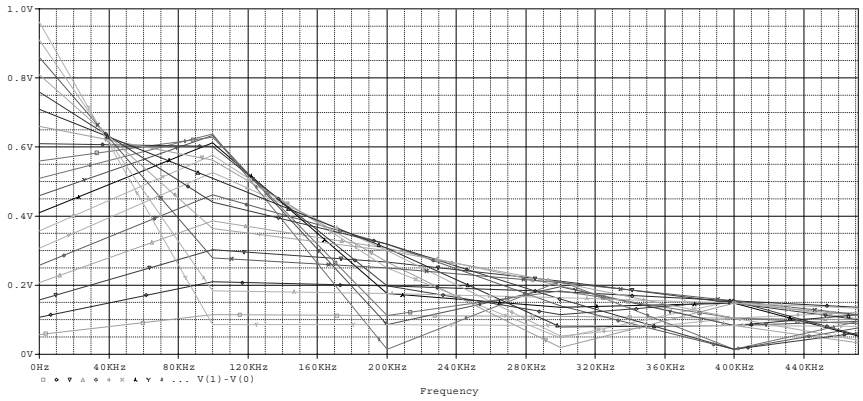



**Figure 3.3** FFT of the .STEP analysis. The waveform with the largest amplitude at 100 kHz corresponds to the 50% duty cycle (TON= 5 $\mu$s).

voltage source. In this case, the pulse has an initial amplitude of 1 V and switches to 0 V after delay "TON." "TON" is swept from 0.5 to 9.5 $\mu$s in 0.5-$\mu$s steps.

When the simulation is finished, you can use Probe to display the X-Y data, or you may view the output file in a text editor. You will have a graph of the fundamental harmonic versus "TON." This confirms the previous statement that the 50% duty cycle was the maxima and provides a reference you may find helpful in the future.

```
X3: .STEP ANALYSIS
.PROBE
.PARAM TON=0.5u
.STEP PARAM TON 0.5u 9.5u 0.5u
.TRAN .1U 10U
.PRINT TRAN V(1)
V1 1 0 PULSE 1 0 {TON}
.END
```

The FFT results of the .STEP analysis are shown in the graphs of Figs. 3.3 and 3.4.

#### Example 4 – EMI filter design

In order to design the EMI filter, we need to define a converter that will operate with it. For the purpose of this example, let us assume that we have a power converter that will operate with an input voltage of 18 to 32 V DC. The converter output power will be 75 W and will have an operating efficiency of 75%. The converter will have a switching frequency of 100 kHz. The conducted emissions requirement allows the 1-mA peak to be reflected back to the input lines. A second-order filter will be used.

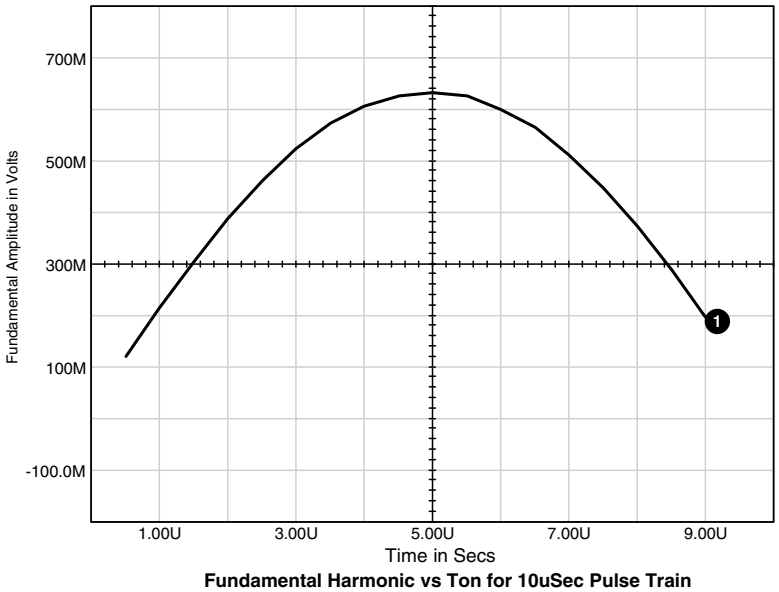



**Figure 3.4** .STEP analysis result shows the 50% duty cycle as the maxima.

Let us follow the procedures that were defined in the EMI design flowchart. Step 1 is to calculate the input impedance.

**Calculating the input impedance.** The input impedance was defined earlier in this chapter as

$$\frac{V_{\text{in}}^2 * \text{efficiency}}{P_{\text{out}}}$$

It is obvious that the lowest impedance will occur at the minimum input voltage. This value can be calculated as

$$\frac{18^2 \times 0.75}{75} = 3.24\,\Omega$$

**Calculating the harmonic content.** Because no detail is provided regarding the pulse current waveforms, we will assume that the duty cycle is 50%. The average input current is

$$I_{\text{avg}} = \frac{P_{\text{out}}}{V_{\text{in}} * \text{efficiency}} = \frac{75}{18 \times 0.75} = 5.56\text{A}$$

At a duty cycle of 50%, the peak amplitude will be 11.12 A. In the previous harmonic analysis, we defined the fundamental harmonic to be $0.636 I_{\text{pk}}$=7.08 A.

**Calculating the required attenuation.** With a maximum reflected ripple current of 1-mA peak, we can define the attenuation required as

$$\text{Attenuation} = \frac{7.08}{0.001} = 7080 = 77 \text{ dB}$$

**Calculating the component values.** The attenuation for a second-order filter can be defined as

$$\text{Attenuation} = \left(\frac{f_{\text{switch}}}{f_{\text{filter}}}\right)^2$$

We can compute the filter frequency as

$$\frac{100 \text{ kHz}}{\sqrt{\text{Attenuation}}} = \frac{100 \text{ kHz}}{84.14} = 1188 \text{ Hz.}$$

The values of $L$ and $C$ can be defined by setting their impedances to the input converter input impedance at the filter resonant frequency, as defined above.

$$C = \frac{1}{2\pi(1188)(3.24)} = 41.35\,\mu\text{F}$$

$$L = \frac{3.24}{2\pi(1188)} 434\,\mu\text{H}$$

Note that the characteristic impedance of the filter is defined by

$$Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{434\,\mu\text{H}}{41.35\,\mu\text{F}}} = 3.24\ \Omega$$

which is equal to the converter input impedance. In an actual design, it is a good practice to provide a 6-dB margin for these characteristics.

## Damping Elements

While this filter provides the proper impedance matching and the required attenuation, the impedance will be quite high at the resonant frequency of the filter. The only damping elements in the circuit are the DC resistance (DCR) of the inductor and the equivalent series resistance (ESR) of the capacitor (which we have not defined). It is normally necessary to provide damping of the L-C filter in order to restrict the impedance of the filter at the resonant frequency. A shunt series R-C network is used for this purpose. The value of the damping capacitor is generally 3 to 5 times greater than that of the filter capacitor, and

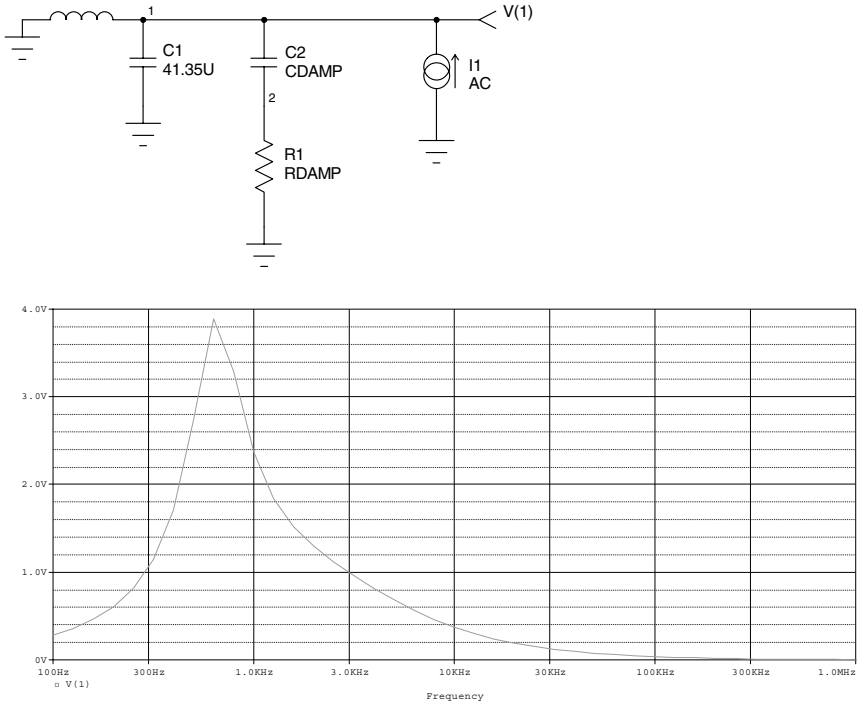



**Figure 3.5** Schematic of the test circuit used to measure the impedance of the filter. The waveform V(1) is equivalent to the impedance because the input is a current (I1 1 0 AC 1). The case for CDAMP = 120$\mu$ and RDAMP = 1.6 is shown.

the value of the damping resistor is generally close to the characteristic impedance of the filter. The PSpice .Step command is ideal for defining these elements.

The following circuit is designed to measure the impedance of the filter, while sweeping the damping capacitor from 120 to 200 $\mu$F in 40-$\mu$F increments. For each value of the damping capacitor, the damping resistor will be swept from 0.5 to 2 times the characteristic impedance (1.6 to 6.4 $\Omega$) in 0.6-$\Omega$ increments. The PSpice listing and schematic of the test circuit (Fig. 3.5) are shown below.

The results are shown below.

```
EX4: TO MEASURE THE IMPEDANCE OF A FILTER
.AC DEC 10 100HZ 1MEGHZ
.PARAM CDAMP=120u
.PARAM RDAMP=1.6
.STEP PARAM CDAMP 120U 200U 40U
.STEP PARAM RDAMP 1.6 6.4 .6
.PROBE
C1 1 0 41.35U
```

```
C2 1 2 {CDAMP}
R1 2 0 {RDAMP}
I1 0 1 AC 1
L1 0 1 434U
.END
```

The results are provided in the output file and are shown below.

Sweep Analysis of EX4.ckt

| Count | CDAMP | RDAMP | Maximum |
|---|---|---|---|
| 1 | 1.20000e-004 | 1.60000e+000 | 3.891 |
| 2 | 1.20000e-004 | 2.20000e+000 | 3.440 |
| 3 | 1.20000e-004 | 2.80000e+000 | 3.557 |
| 4 | 1.20000e-004 | 3.40000e+000 | 3.916 |
| 5 | 1.20000e-004 | 4.00000e+000 | 4.395 |
| 6 | 1.20000e-004 | 4.60000e+000 | 4.840 |
| 7 | 1.20000e-004 | 5.20000e+000 | 5.248 |
| 8 | 1.20000e-004 | 5.80000e+000 | 5.619 |
| 9 | 1.20000e-004 | 6.40000e+000 | 6.104 |
| 10 | 1.60000e-004 | 1.60000e+000 | 2.994 |
| 11 | 1.60000e-004 | 2.20000e+000 | 2.869 |
| 12 | 1.60000e-004 | 2.80000e+000 | 3.153 |
| 13 | 1.60000e-004 | 3.40000e+000 | 3.672 |
| 14 | 1.60000e-004 | 4.00000e+000 | 4.161 |
| 15 | 1.60000e-004 | 4.60000e+000 | 4.614 |
| 16 | 1.60000e-004 | 5.20000e+000 | 5.033 |
| 17 | 1.60000e-004 | 5.80000e+000 | 5.580 |
| 18 | 1.60000e-004 | 6.40000e+000 | 6.121 |
| 19 | 2.00000e-004 | 1.60000e+000 | 2.489 |
| 20 | 2.00000e-004 | 2.20000e+000 | 2.593 |
| 21 | 2.00000e-004 | 2.80000e+000 | 3.024 |
| 22 | 2.00000e-004 | 3.40000e+000 | 3.547 |
| 23 | 2.00000e-004 | 4.00000e+000 | 4.038 |
| 24 | 2.00000e-004 | 4.60000e+000 | 4.494 |
| 25 | 2.00000e-004 | 5.20000e+000 | 5.040 |
| 26 | 2.00000e-004 | 5.80000e+000 | 5.591 |
| 27 | 2.00000e-004 | 6.40000e+000 | 6.137 |

The impedance was exceeded with the 120-$\mu$F damping capacitor (Fig. 3.6). If we use a 160-$\mu$F capacitor, the impedance will be minimized with a 2.2-$\Omega$ damping resistor. A lower impedance could be achieved with a 200-$\mu$F damping capacitor and a 1.6-$\Omega$ damping resistor. We will select the 160-$\mu$F capacitor and the 2.2-$\Omega$ resistor.

The following simulation shows the impedance characteristics and the reflected ripple of the filter (see also Figs. 3.7 and 3.8).

```
EMI2: TO SHOW THE REFLECTED RIPPLE OF THE FILTER
.AC DEC 10 100HZ 100KHZ
.TRAN 1U 10M 9980U .1u UIC
.PROBE
```

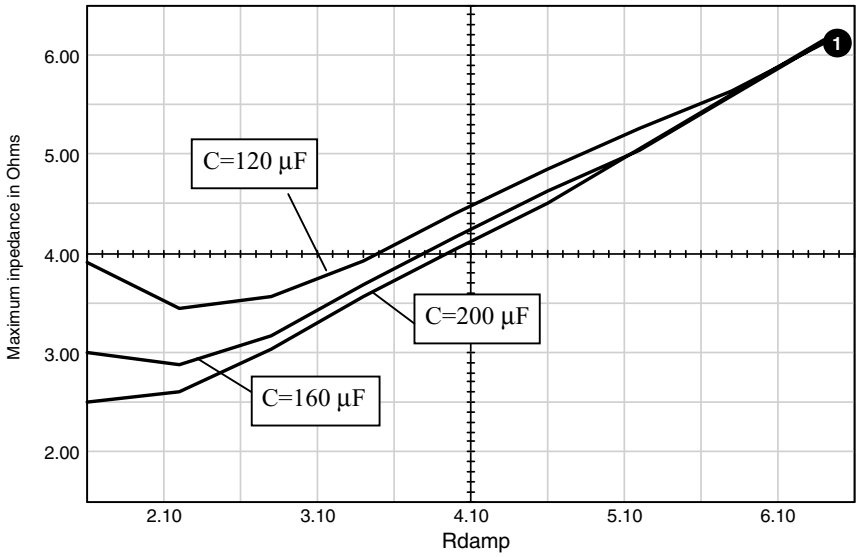



**Figure 3.6** Family of curves showing the maximum impedance versus the damping resistor value. Each curve represents a different capacitor value.

```
C1 2 0 41.35U
C2 2 1 160U
R1 1 0 2.2
I1 0 2 AC 1 PULSE 0 11 0.1U 0.1U 0.1U 5U 10U
L1 0 2 434U IC=-5.5
.END
```

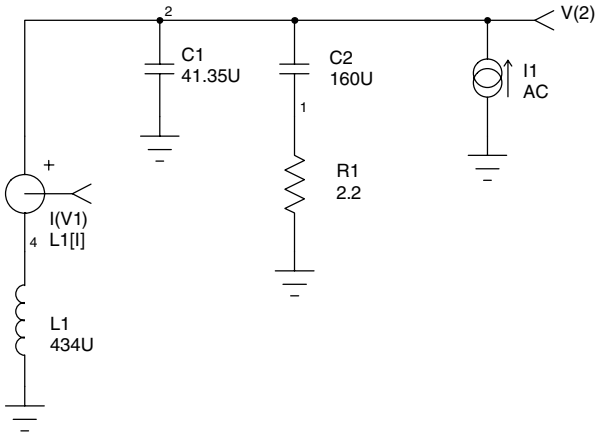
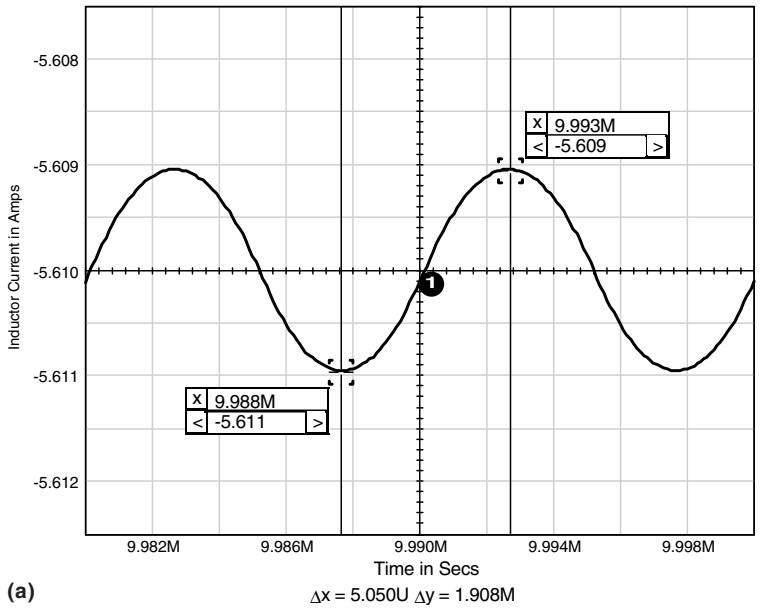



**Figure 3.7** Circuit used to show the impedance and the reflected ripple of the filter.



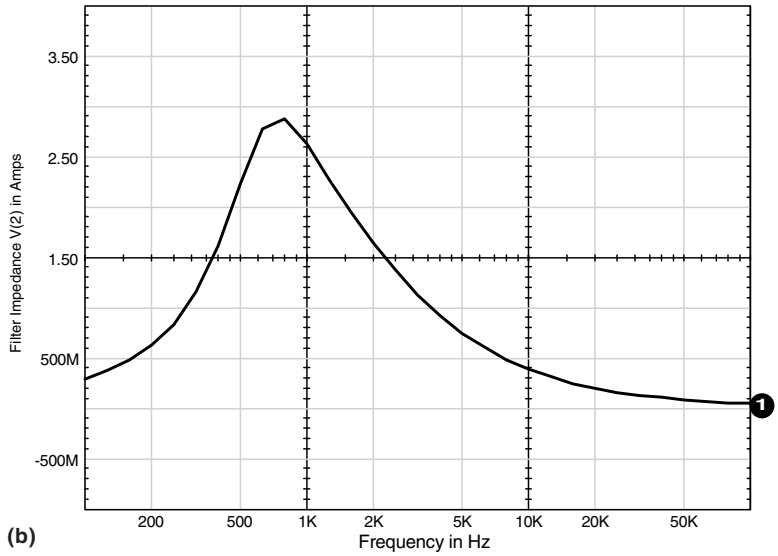




**Figure 3.8** Current in the inductor ***(a)*** due to a current pulse input, and impedance characteristics over frequency ***(b)*** for the filter circuit in Fig. 3.7.

## Fourth-Order Filters

Because the physical size of power converters is continually shrinking, higher order filters are being used more often than not. The filter is

designed in much the same way as the second-order filter. The following example demonstrates the design of a fourth-order filter using the same design parameters as those that we used for the previous filter.

The "octave" rule basically states that resonances should be at least an octave apart. In an effort to be conservative, let us use a factor of 2.5. The attenuation of the filter can be defined as

$$\text{Attenuation} = \left(\frac{f_{\text{switch}}}{f_1}\right)^2 * \left(\frac{f_{\text{switch}}}{2.5\,f_1}\right)^2 = \frac{f_{\text{switch}}^4}{6.25\,f_1^4}$$

If we set the attenuation at 7080, as in the previous example, and solve for $f_1$ we obtain $f_1$=6.895 kHz. The second pole is then at $2.5\,f_1 =$ 17.237 kHz.

The impedance of each section should be designed to be lower than the impedance of the converter, which we had determined to be 3.24 Ω in the previous example. The filter is loaded by the negative resistance of the converter and produces a combined impedance of

$$Z_{\text{loaded}} = \frac{Z_{\text{in}} * Z_{\text{o}}}{Z_{\text{in}} + Z_{\text{o}}}$$

The loaded filter $Q$ is defined as

$$Q = \frac{Z_{\text{loaded}}}{Z_{\text{o}}}$$

where $Z_{\text{o}}$ is the filter characteristic impedance defined by

$$Z_{\text{o}} = \sqrt{\frac{L}{C}}$$

If we combine the above equations, we have

$$Q = \frac{Z_{\text{in}} * Z_{\text{o}}}{(Z_{\text{in}} + Z_{\text{o}})\,Z_{\text{o}}}$$

$$Z_{\text{o}} = -\left(\frac{Q-1}{Q}\right) Z_{\text{in}}$$

The filter $Q$ is generally maintained below a value of 2. If we set $Q = 2$ and solve for $Z_{\text{o}}$ we obtain

$$Z_{\text{o}} = -\left(\frac{2-1}{2}\right)(-3.24) = 1.62\ \Omega$$

If we use this impedance and the calculated resonant frequencies, we can define both inductors and both capacitors.

$$L_1 = \frac{1.62}{2\pi\ (6895)} = 37\ \mu\text{H}$$

$$C_1 = \frac{1}{2\pi\ (6895)\,(1.62)} = 14\ \mu\text{F}$$

$$L_2 = \frac{1.62}{2\pi\ (17,237)} = 15\ \mu\text{H}$$

$$C_2 = \frac{1}{2\pi\ (17,237)\,(1.62)} = 5.7\ \mu\text{F}$$

As shown in the previous example, we can use the .Step command to sweep the values of the damping capacitor and the damping resistor. If we use a range of 3 to 5 times the value of the real capacitor, we will sweep the damper capacitor from 42 to 70 $\mu$F in steps of 14 $\mu$F. We will sweep the damper resistor from one-half to twice the $Z_o$ of the filter, i.e., from 0.8 to 3.2 Ω in 0.2-Ω steps.

The schematic for the fourth-order filter and its impedance response are shown in Fig. 3.9.

Note that two 10-MΩ resistors have been added. To aid circuit convergence, the resistors were added to the nodes that are purely reactive. The circuit listing and output file are shown below. A sweep of the maximum impedance as a function of the damping resistor and the damping capacitor was also performed. The results of the sweep are shown in Fig. 3.10. Each curve is for a different value of damping capacitor.

```
4THORD: A 4TH ORDER FILTER
.AC DEC 10 100HZ 1MEGHZ
.PROBE
.PARAM CDAMP=42u
.PARAM RDAMP=0.8
.STEP PARAM CDAMP 42U 70U 14U
*.STEP PARAMRDAMP .8 3.2 .2
.PRINT AC V(4) VP(4)
1 1 0 5.7U
C2 4 2 {CDAMP}
R1 2 0 {RDAMP}
I1 0 4 AC 1
L2 1 4 37U
C3 4 0 14U
R2 1 0 10MEG
R3 4 0 10MEG
L1 0 1 15U
.END
```

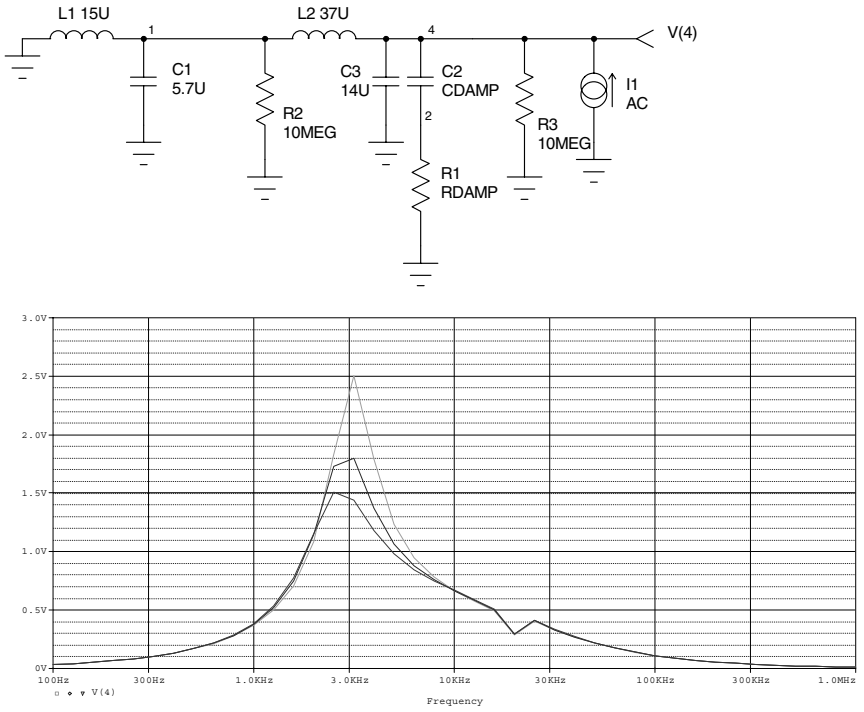



**Figure 3.9** Fourth-order filter schematic and impedance response.

| Count | CDAMP | RDAMP | Maximum |
|---|---|---|---|
| 1 | 4.20000e-005 | 8.00000e-001 | 2.507 |
| 2 | 4.20000e-005 | 1.00000e+000 | 2.215 |
| 3 | 4.20000e-005 | 1.20000e+000 | 2.027 |
| 4 | 4.20000e-005 | 1.40000e+000 | 2.024 |
| 5 | 4.20000e-005 | 1.60000e+000 | 2.083 |
| 6 | 4.20000e-005 | 1.80000e+000 | 2.133 |
| 7 | 4.20000e-005 | 2.00000e+000 | 2.285 |
| 8 | 4.20000e-005 | 2.20000e+000 | 2.458 |
| 9 | 4.20000e-005 | 2.40000e+000 | 2.627 |
| 10 | 4.20000e-005 | 2.60000e+000 | 2.791 |
| 11 | 4.20000e-005 | 2.80000e+000 | 2.950 |
| 12 | 4.20000e-005 | 3.00000e+000 | 3.103 |
| 13 | 5.60000e-005 | 8.00000e-001 | 1.799 |
| 14 | 5.60000e-005 | 1.00000e+000 | 1.716 |
| 15 | 5.60000e-005 | 1.20000e+000 | 1.659 |
| 16 | 5.60000e-005 | 1.40000e+000 | 1.727 |
| 17 | 5.60000e-005 | 1.60000e+000 | 1.820 |
| 18 | 5.60000e-005 | 1.80000e+000 | 1.979 |
| 19 | 5.60000e-005 | 2.00000e+000 | 2.158 |
| 20 | 5.60000e-005 | 2.20000e+000 | 2.334 |
| 21 | 5.60000e-005 | 2.40000e+000 | 2.505 |
| 22 | 5.60000e-005 | 2.60000e+000 | 2.670 |

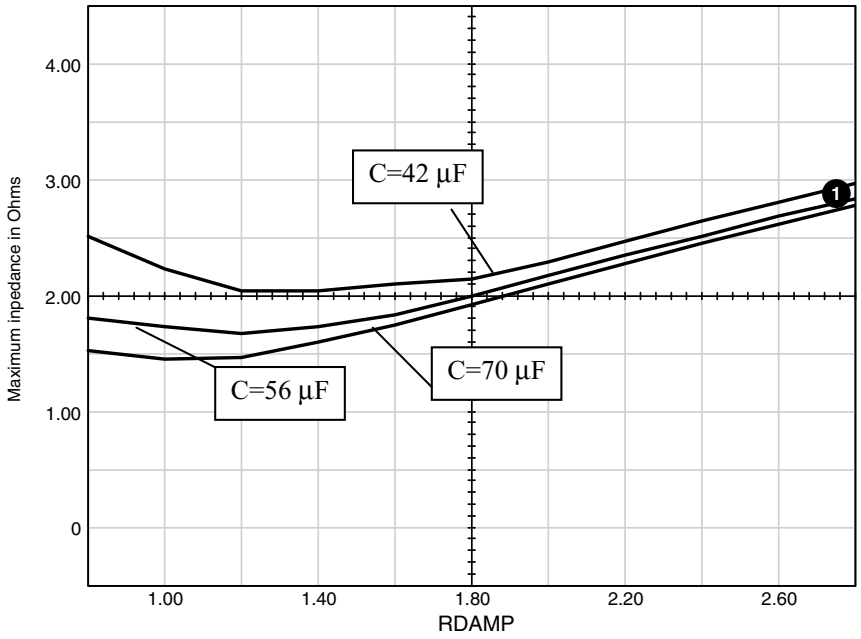



**Figure 3.10** Family of curves showing the maximum impedance of the fourth-order filter.

| | | | |
|---|---|---|---|
| 23 | 5.60000e-005 | 2.80000e+000 | 2.830 |
| 24 | 5.60000e-005 | 3.00000e+000 | 2.985 |
| 25 | 7.00000e-005 | 8.00000e-001 | 1.512 |
| 26 | 7.00000e-005 | 1.00000e+000 | 1.448 |
| 27 | 7.00000e-005 | 1.20000e+000 | 1.461 |
| 28 | 7.00000e-005 | 1.40000e+000 | 1.582 |
| 29 | 7.00000e-005 | 1.60000e+000 | 1.728 |
| 30 | 7.00000e-005 | 1.80000e+000 | 1.913 |
| 31 | 7.00000e-005 | 2.00000e+000 | 2.093 |
| 32 | 7.00000e-005 | 2.20000e+000 | 2.269 |
| 33 | 7.00000e-005 | 2.40000e+000 | 2.440 |
| 34 | 7.00000e-005 | 2.60000e+000 | 2.606 |
| 35 | 7.00000e-005 | 2.80000e+000 | 2.767 |
| 36 | 7.00000e-005 | 3.00000e+000 | 2.922 |

As evident from the data, we could "squeak by" with the 56-$\mu$F damper or conservatively use the 70-$\mu$F value. We will use 68 $\mu$F, which is the nearest standard value to 70 $\mu$F. The damper resistance is optimum at 1 Ω. *Note: The 1-Ω value includes the ESR of the capacitor, so select the resistor value less than the ESR value of the capacitor*. The results of our new filter simulation are shown in Fig. 3.11.

The attenuation is very close to the desired 77-dB limit, and the impedance is well below the 3.24-Ω stability requirement. Notice the

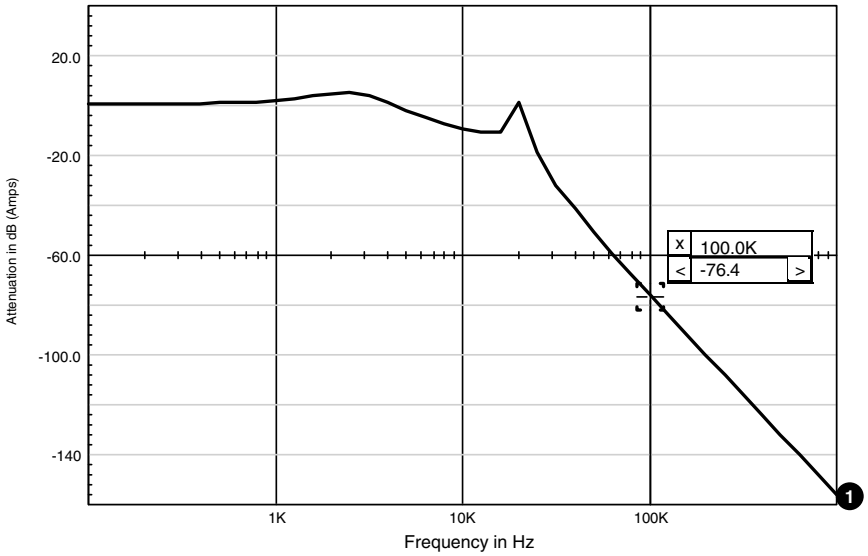



**Figure 3.11** The filter attenuation using the optimized values for the damper section.

peaking of the undamped first stage of the filter. The .STEP analysis may be used to determine optimum values for the damper section also, if desired. We will use the same capacitor ratio as we had determined for the second stage. This yields a damper capacitor value of approximately 33 $\mu$F, and we will use the same 1-$\Omega$ value for the damper resistor. While we are at it, let us change the 5.7-$\mu$F capacitor to 6.8 $\mu$F in order to obtain a standard value and to slightly improve the attenuation. Notice that the peaking of the first stage has nearly been eliminated, and the attenuation has been improved to meet the requirement of 77 dB (Fig. 3.12).

## Inrush Current

In many applications, the input voltage is applied as a step. This may be the result of a switch or relay closure. The current that is drawn by the filter during this application of power is referred to as the inrush current. The inrush current may be of concern, because of stress or fuse ratings. We can evaluate the inrush characteristics of our filter by applying a step input from 0 V to the maximum input voltage (32 V in our design) while monitoring the current that is drawn by our filter.

Note that we can use the same model for both the AC and transient analyses. The results of the inrush current simulation are shown in Fig. 3.13. The inrush current has a peak value of 34 A. The output voltage

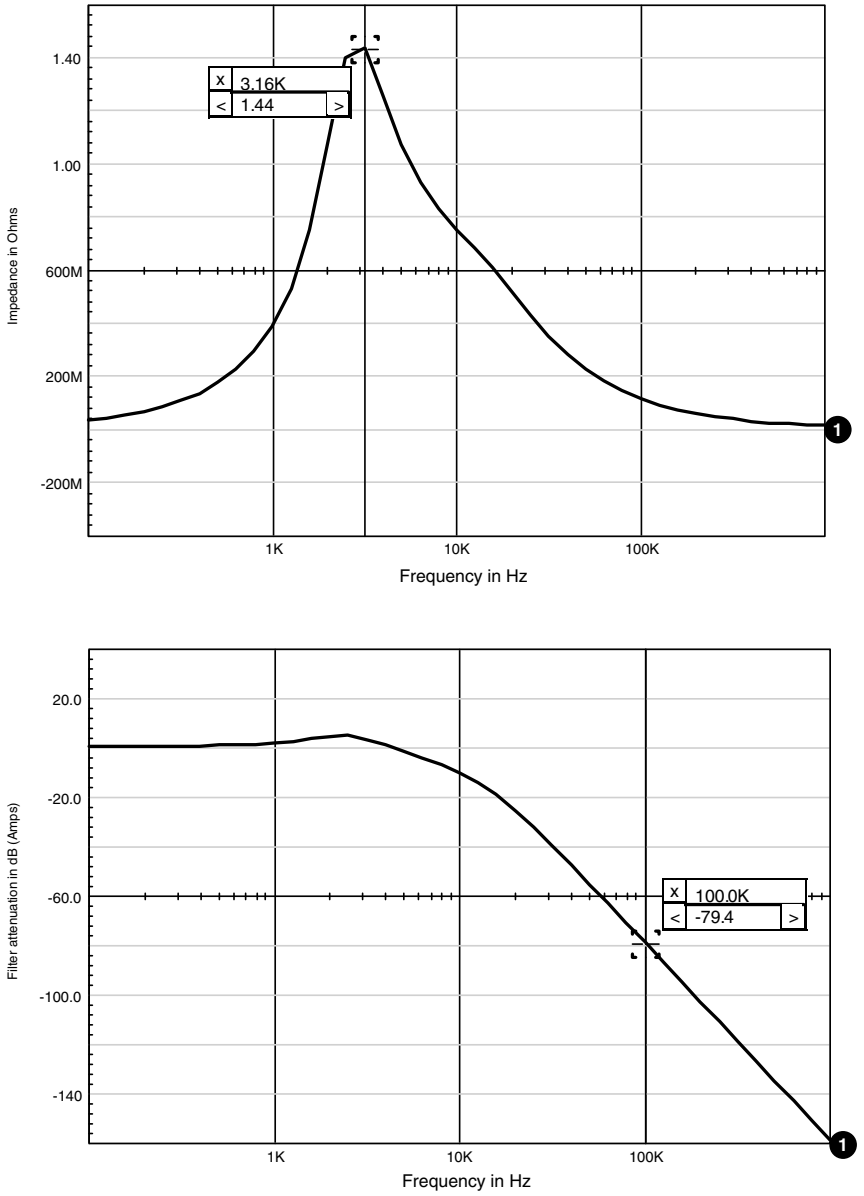



**Figure 3.12** The filter attenuation graph shows the elimination of the peaking in the first stage after changes in the damper section.

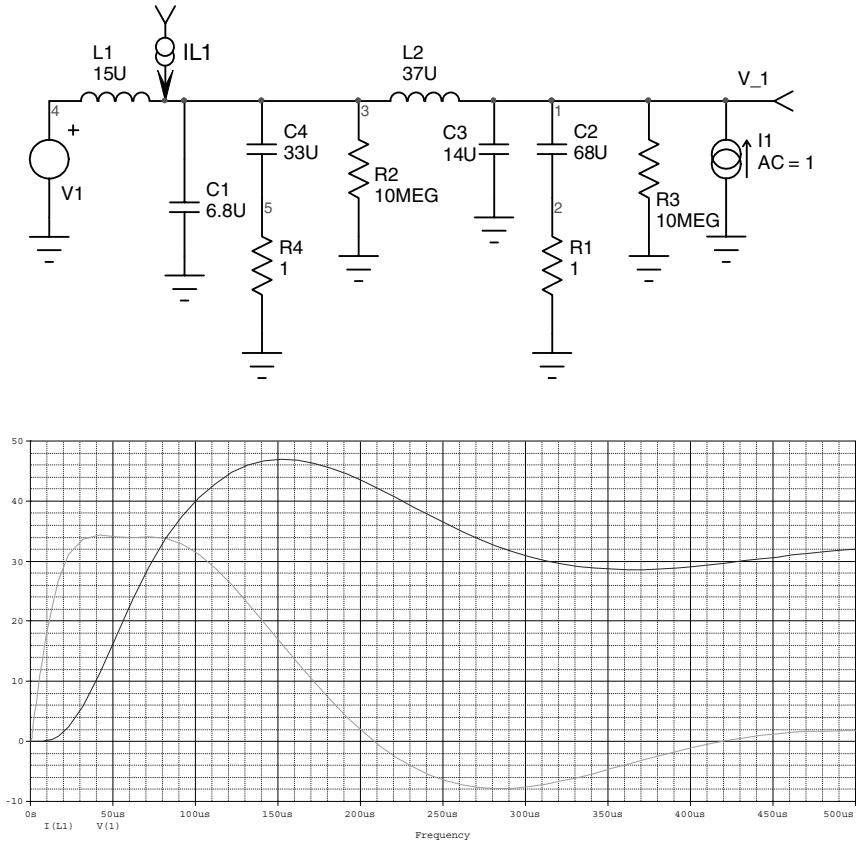



**Figure 3.13** Schematic, netlist, and simulation results for the inrush current simulation.

of the filter is also displayed. When a 32-V step voltage was applied, the filter output overshot to almost 48 V. This is an important consideration for selecting and derating the components that are used in the switching converter that follows the filter.

```
4THORD2.cir
.AC DEC 10 100 1meg
.TRAN 1u 500u
.PROBE
C2 1 2 68U
C3 1 0 14U
R1 2 0 1
R2 3 0 10MEG
R3 1 0 10MEG
L1 4 3 15U
L2 3 1 37U
I1 0 1 AC=1
```

```
V1 4 0 PULSE 0 32
C1 3 0 6.8U
C4 3 5 33U
R4 5 0 1
.END
```

### MPP Inductors

The previous example utilized ideal inductors. In real applications, however, the inductors generally do not provide a constant inductance. Rather, they tend to saturate as current is passed through them. One of the more popular cores used in these applications is Magnetics® MPP style.

Using MPP cores for our EMI filter provides a more realistic model than the ideal inductor model. The following simulations use a Magnetics 55131 core with 29 turns for the 15-$\mu$H inductor and a Magnetics 55121 core with 36 turns for the 37-$\mu$H inductor (Fig. 3.14). DC resistances are 0.035 Ω and 0.025 Ω, respectively. Note the third terminal on the inductor symbol. The extra terminal is used to monitor the instantaneous inductance value.

```
4THINRS3.cir
.PROBE
.AC DEC 10 100 1meg
.TRAN .1u 500u 0 .5u
C2 2 3 68U
C3 2 0 14U
R1 3 0 1
C4 1 7 33U
R2 1 0 10MEG
R3 2 0 10MEG
R4 7 0 1
I1 0 2 AC=1 ; DC=-4.5 used for Figure 3.16
X1 6 1 8 MP55131 Params: N=29 DCR=.035 IC=0
X2 1 2 9 MP55121 Params: N=36 DCR=.035 IC=0
V1 4 0 PULSE 0 32
V2 4 6
C1 1 0 6.8U
.END
```

This simulation also calculates the attenuation and impedance of the filter without DC current using the AC analysis (Fig. 3.15).

If we add a DC current value of 4.5 A (100 W/22 V), we will see the data for the filter as it operates under full load conditions. The inductance of each MPP core can be monitored using markers as the simulation progresses. The schematic will provide the values at the steady state condition. If we view the inductance, we will see the value of inductance during the inrush current.

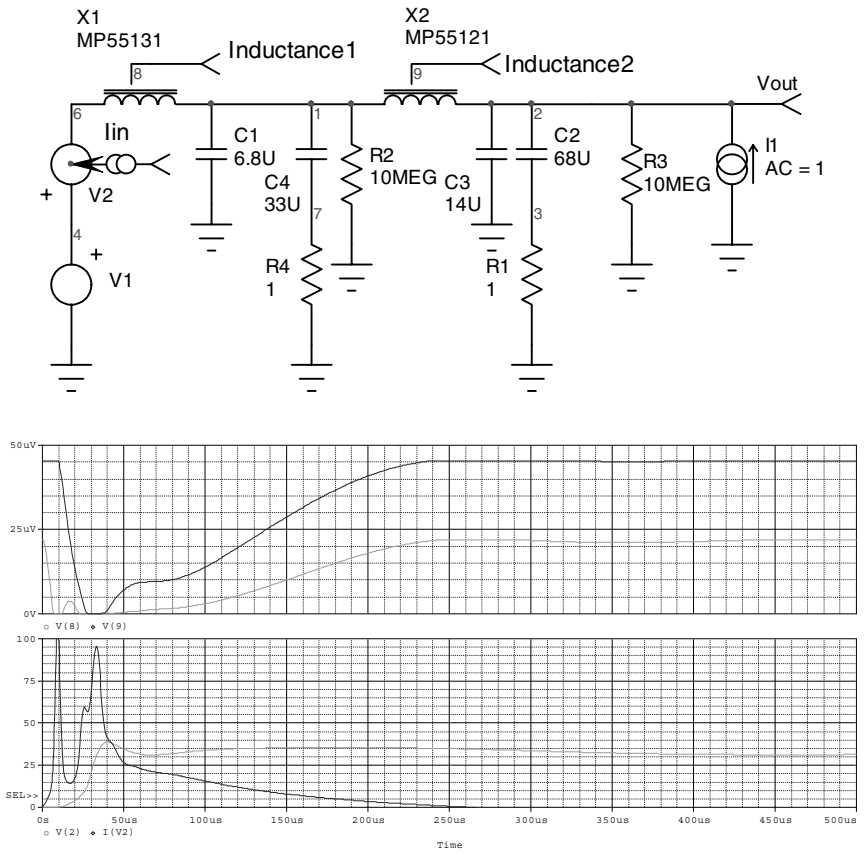



**Figure 3.14** A more realistic simulation using MPP cores for EMI filter design. The instantaneous inductance is shown for both MPP cores (top graph) and for the input current and output voltage.

The first simulation in Fig. 3.14 showed the results of the simulation without DC current. As you can see, the inrush current is considerably higher than the value we expected in the first simulation. This is due to the saturation of the inductors. The waveforms in Fig. 3.14 show the inductance during the inrush current.

The input inductor is almost completely saturated by the inrush current. The inductance value in the schematic is somewhat higher than the design value.

The second simulation in Figs. 3.16 and 3.17 shows the results of the simulation with a DC value of 4.5 A added to the current source I1.

The current is negative because of the direction of the current source. The inductor values are almost identical to the design values. The inrush current analysis has not been performed, because it is unrealistic

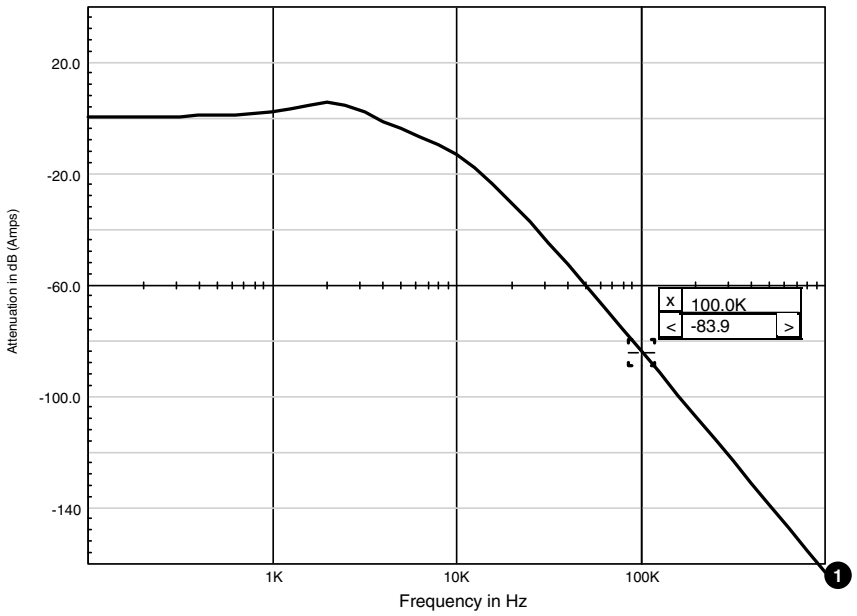



**Figure 3.15** Simulation result of the attenuation without a DC current.

to have the 4.5-A current flowing when the converter is turned on. The attenuation analysis was performed, and the results are shown in Fig. 3.17.

The attenuation has been degraded by approximately 4 dB as a result of the DC current; however, it is still sufficient to meet the 77-dB requirement.

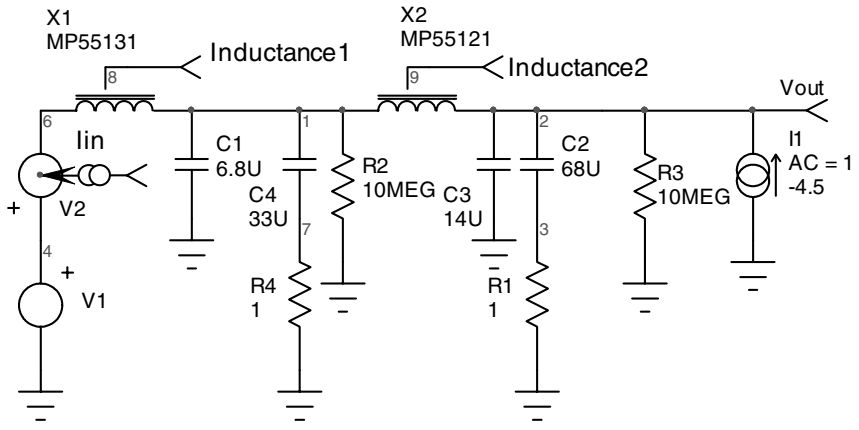



**Figure 3.16** A realistic model using MPP cores with a 4.5-A steady state current.

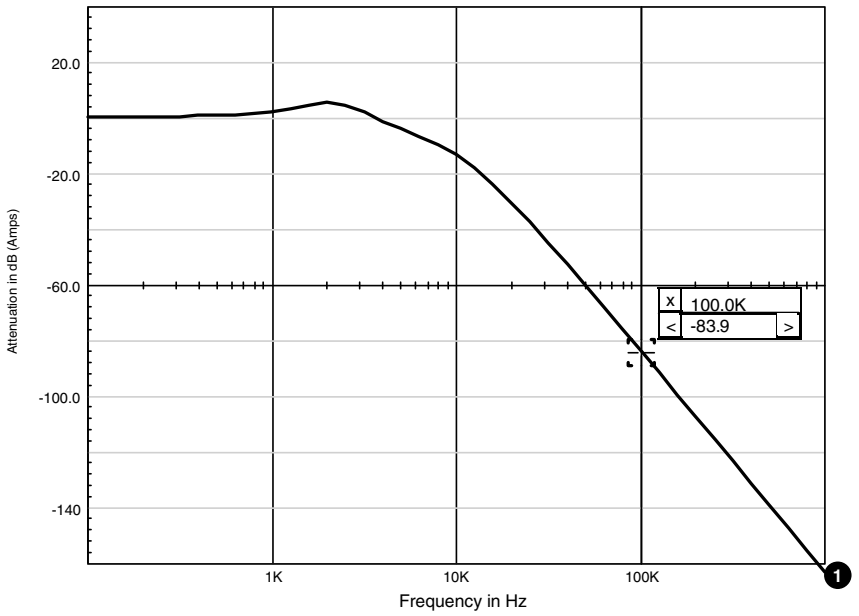



**Figure 3.17** Effect of the DC current on the attenuation analysis.

The inrush current simulation is one of the most difficult simulations to correlate with real hardware. This is generally due to the effects of the source impedance of the test setup. Keep in mind that the power supplies and cables have resistance and inductance. The SPICE model must account for these elements, or they must absolutely be minimized. With this in mind, it is certainly feasible to get good correlation with a little care.

The example circuit in Fig. 3.18 was constructed for the purpose of determining the accuracy of the model. The 28.8-$\mu$H input inductor is constructed as 24 turns on a 58271 core, and the two 25.1-$\mu$H inductors are constructed as 28 turns on two stacked 58291 cores. The results are shown in Figs. 3.19 and 3.20. The inductance of these two inductors is shown in Fig. 3.18. Note that the input inductor drops by more than 60% as a result of the inrush current.

```
emi inrush correlation.cir
.PROBE
.TRAN 10n 250u 0 50n
C2 10 11 3U
C3 9 2 1U
R1 11 0 4.99
R2 2 0 4.99
C4 9 0 1U
X1 9 7 3 MP58291 Params: N=28 DCR=.13 IC=0
```

```
X2 7 10 6 MP58291 Params: N=28 DCR=.13 IC=0
X3 1 9 8 MP58271 Params: N=24 DCR=.1 IC=0
V1 4 1 DC=0
V2 4 0 PULSE 0 28 50u .1U .1U 100M 200M
C1 10 0 1U
.END
```

The correlation results are excellent despite the saturation of the input inductor.

## Inrush Current Limiting

Some circuits are sensitive to the level of inrush current. In order to limit this current, two basic possibilities exist: the input inductors can be oversized in order to prevent saturation, or an inrush limiting scheme can be used.

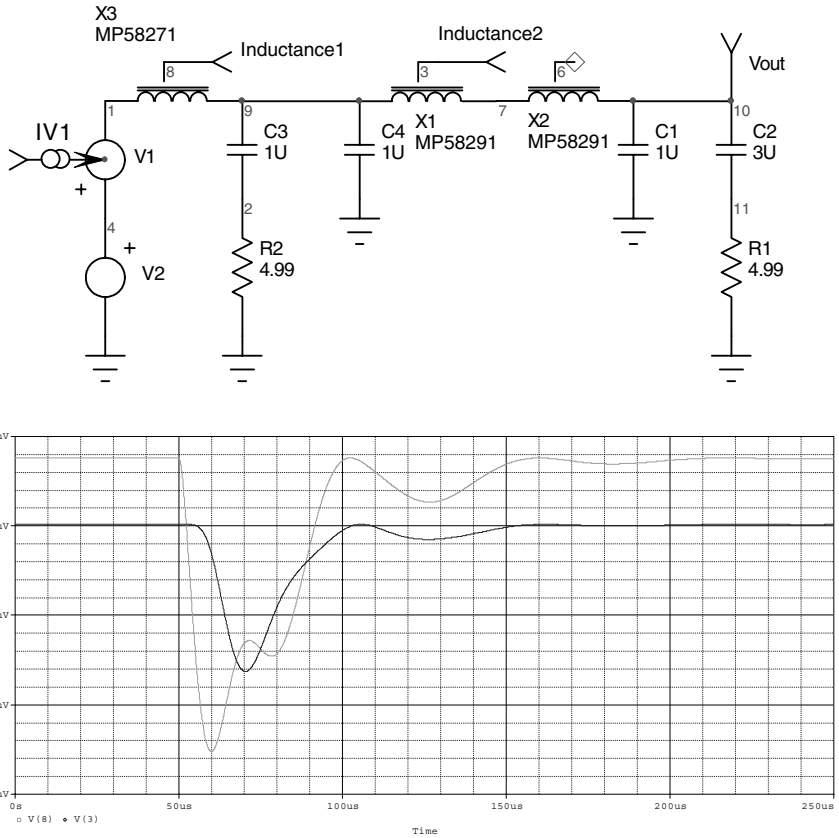



**Figure 3.18** EMI filter constructed for inrush correlation. Inductance of the cores is shown over time.

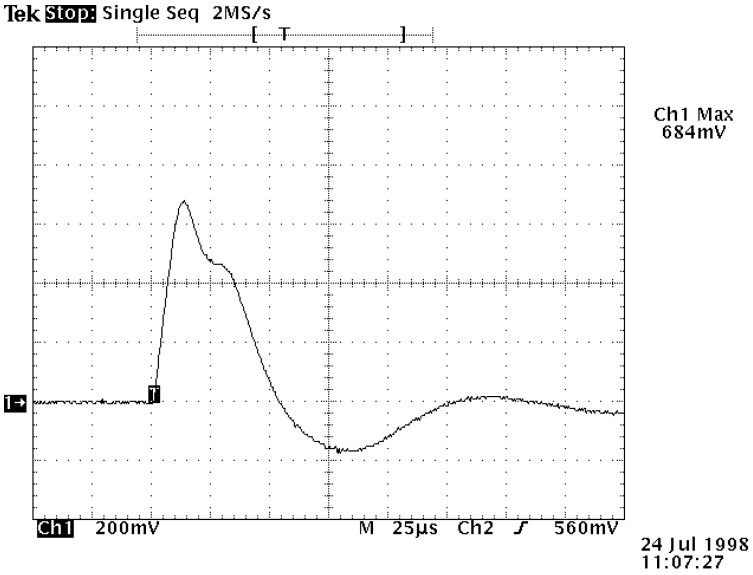



**Figure 3.19** Inrush measured result.

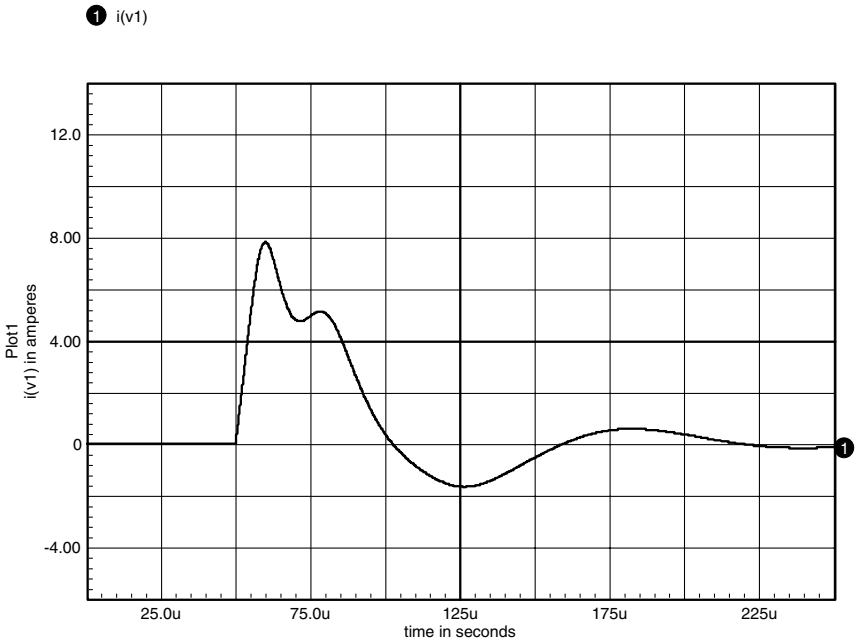



**Figure 3.20** Inrush simulated result.

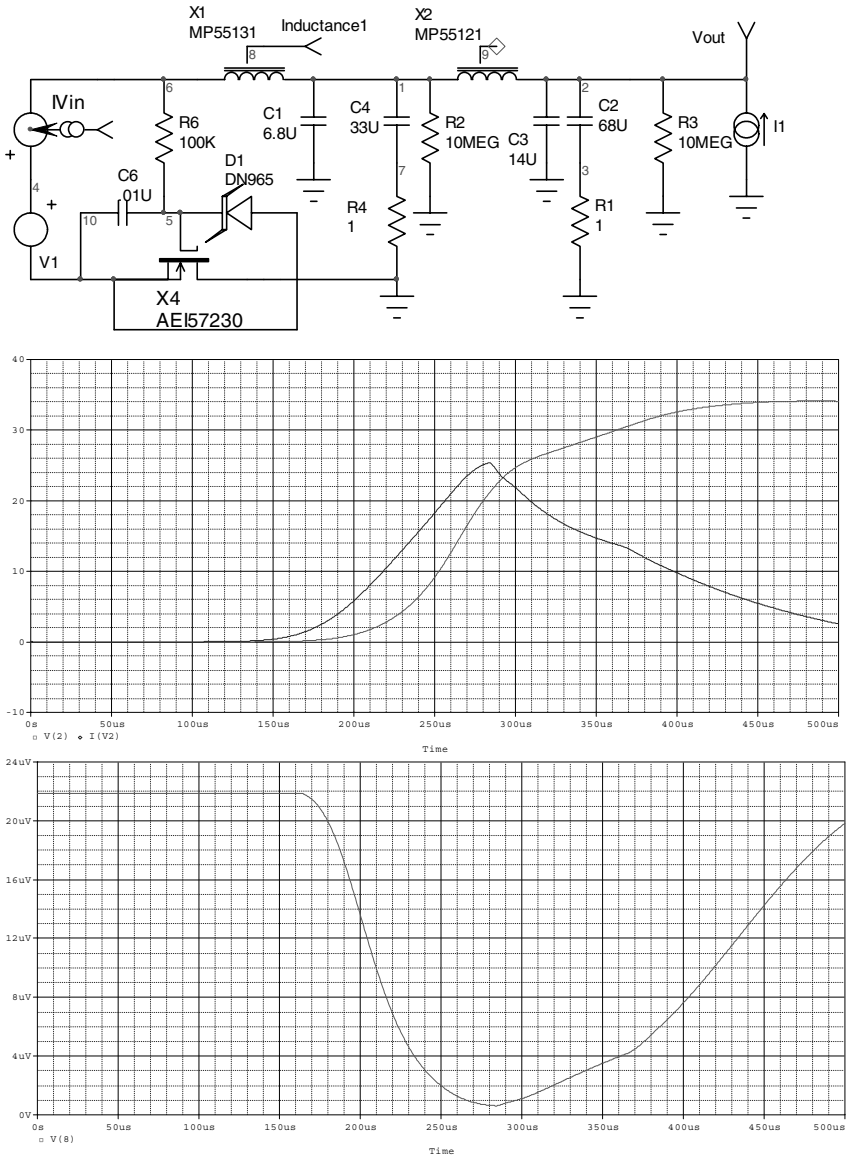



**Figure 3.21** A filter design using a MOSFET inrush current limiter scheme.

Many schemes have been used as effective inrush current limiters. Some of the more popular schemes are as follows:

- Add a relay or SCR across a current-limiting resistor. This allows the filter capacitors to charge through a limiting resistor and then shorts the resistor after the input capacitors are charged.

- Solid-state devices such as MOSFETs can be used to limit the input filter's dv/dt in order to limit the current.
- Use resistors with a negative temperature coefficient. These devices are commercially available and provide a limiting resistance at turn-on. Once they are loaded, the resistors heat up and drastically reduce in value.

As a final example, let us simulate an inrush current limiting scheme. The following schematic shows the addition of a MOSFET inrush limiter. The zener diode limits the gate voltage to 15 V, which is well below the 20-V rating. If the zener were not present, the gate voltage would charge to the input voltage and damage the MOSFET.

```
INRSHLMT.cir
.PROBE
.TRAN 1u 500u 0 .5u
C2 2 3 68U
C3 2 0 14U
R1 3 0 1
C4 1 7 33U
R2 1 0 10MEG
R3 2 0 10MEG
C6 5 10 .01U
R4 7 0 1
R6 6 5 100K
I1 0 2 AC=1
X1 6 1 8 MP55131 {N=29 DCR=.035 IC=0}
X2 1 2 9 MP55121{N=36 DCR=.035 IC=0}
V1 4 10 PULSE 0 32
V2 4 6
C1 1 0 6.8U
.END
```

The waveforms show the inrush current with the addition of the MOSFET limiter. Different values of R6 and C6 will produce different results; however, this is adequate in order to demonstrate the concept. The selected MOSFET has an $R_{ds_{on}}$ that limits the power dissipation to an acceptable value.

Other implementations of inrush current limiting use negative temperature coefficient (NTC) thermistors designed specifically for this application. Resistor inrush limiters, which are bypassed using an SCR or a relay after the initial inrush, are also fairly common. In this case it is important to assure that the load on the filter is not applied until *after* the bypass device is enabled; otherwise, the input filter may not fully charge, resulting in a second inrush when the bypass device is enabled.