How To Reduce EMC Problems On Your Design

a. Critical nets must not cross a split in the adjacent reference plane.
b. Critical nets must not change reference planes.
c. Critical nets may not be within a specified distance of the edge of their reference plane.
d. Critical nets may not be routed within a specified distance from an I/O net.
e. All critical nets must be buried between solid planes. The allowable length of the exposed portion of a critical net may be specified.
f. All critical nets must have a "ground-guard" trace on either side of the critical net.
g. All differential critical nets must have a "ground-guard" trace on either side of the differential pair of nets.
h. All differential critical nets must be routed within a specified distance of each other, and the length of the differential pair of nets must match within a specified amount.
i. All power and ground traces longer than a specified distance must be wider than another specified distance. This does not include grounded guard traces.
j. Decoupling capacitors must be placed between all adjacent plane pairs within a specified grid density.
k. A decoupling capacitor must be connected between the power and ground-reference planes and be placed within a specified distance from each IC power pin.
l. The trace connecting between the IC power and/or ground reference pin to the associated via to the power/ground-reference plane must be no longer than the specified distance.
m. The trace connecting between a decoupling capacitor to the associated via to the power/ground-reference plane must be no longer than the specified distance.
n. All power and ground-reference traces longer than a specified length must have a decoupling capacitor within a specified distance from the IC power pin.
o. All I/O filters must be placed within a specified distance from the I/O connector.
p. All oscillators must be placed within a specified distance from the clock driver (or other device) that they drive.