Impedance modelling on multiple dielectric builds

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Abstract
As printed circuit board (PCB) track geometries shrink, sometimes it becomes necessary to look deeper than the material data sheet when modelling electrical properties of transmission lines; this study looks at how variation in dielectric constant should be handled in multiple and single dielectric PCB builds. This paper describes how even FR4 builds should in some cases be treated as multiple dielectric builds. Approaches for understanding the root cause of effective dielectric constant variation with structure, coupling and scale are considered. An outline of the implementation of the boundary element method is provided for those wishing to look a little deeper into the modelling process. Finally, a brief investigation covers the sources of measurement errors aimed at helping to put the best data back into the modelling process.

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1. Introduction

Laminate suppliers are increasingly questioning why printed circuit board (PCB) fabricators deviate from the specified dielectric constant in the materials data sheet, often posing the question that if this is necessary there must be some limitations in modelling software. However, what they have missed is the fact that as geometries shrink, effects of the material constituents increasingly come into play when modelling impedance. A good fabricator needs to deviate from the supplier's data, as the material vendor supplies data for the bulk material. Small geometry impedance controlled structures are exposed to small scale effects, and currently designers find that even though the base material has one bulk dielectric constant, the particular structure experiences the electrical properties of a higher component of one constituent part of the laminate. A tightly coupled differential pair on FR4, for example, may experience itself in an environment that is very rich in resin. In addition, some prepregs are double resin coated to obtain a smooth surface finish, thus behaving as though a pure resin layer is floated on the top surface of the board. Employing field solvers based on the boundary element method (BEM) enables the modelling of a wide range of alternative builds and allows the user to consider resin layers, resin rich areas between edge coupled and coplanar structures, and at a more fundamental level, model the use of differing substrate types within the PCB stack up.

2. Using more than one material type in the stack

Essential in the drive to cost-effective high performance PCBs is the move to employ multiple dielectric substrates. This allows a low cost base material to be used for non-critical layers while layers with demanding requirements for speed and signal integrity employ a more suitable high frequency material. This paper describes above some important considerations when employing multiple dielectric builds, and also considers whether multiple dielectric modelling tools can assist in extracting the most from builds constructed of one base material. The key to this study is that when one examines the task of impedance prediction closely, there is more information that needs consideration than would normally appear on the base material data sheet.

2.1 Effective dielectric constant (Er) change from structure to structure: Er – is not always what it says on the data sheet

2.1.1 Bulk and localised structure dependant Er

The dielectric constant value quoted is not always as stated on the manufacturer's data sheet. This is not a problem with the data from the laminate supplier since the figure they offer is the "bulk" Er of the material. What a laminate vendor cannot be expected to define is precisely how the material will behave on the particular board being built. This should not really be a surprise, but all too often is. Consider the field patterns described earlier and the material that the field experiences as it develops in the substrate. The structure of the material, the prepreg, is a mix of resin and glass, and during pressing the resin will flow into the gaps between and adjacent to the traces. There will be a local variation of Er, and in differential structures the impedance may be higher than predicted. Is this a laminate problem? No, one simply needs to understand the material behaviour as it relates to the transmission line structure being employed. There are ways of lessening this effect, using random "Aramid" reinforcement for example, but as in all production situations, cost and manufacturability need to be balanced with performance requirements.

2.2 All builds are at some point "multiple dielectric"

While most engineers would consider a multiple dielectric build as one composed of quite different core and prepreg base materials, the same is true of FR4. This is because the base material is composed of two materials with very different electrical properties, resin with an Er of around 3 and glass with Er of approximately 6. Now that traces are reducing to a similar scale as the constituent materials, the base material should no longer be assumed as homogeneous. It may be thought that this issue can be overcome by employing a higher performance base material, however, while the material remains a mix of glass and resin, the same will still be true. In fact, if one takes the extreme case of a woven glass PTFE material, there is even more variation between the glass Er and the dielectric constant of the PTFE. This is not a problem while the track widths are significantly larger than the dimensions of the glass weave, but when the trace width reduces, this needs to be considered.

2.3 A more detailed look at how the electric field sees the above substrates

First consider Figure 1. The case of coupled lines as shown in this figure is always more challenging from a modelling perspective, as there is a significant field between the differential pair. This field only experiences pure resin between the traces. It is vital that fabricators keep modelling and testing for impedance, then learn the behaviour of each structure and geometry range for use in future similar builds. These data will increase the chance of higher first time yields.

Figure 2 clearly shows the differing materials surrounding the traces, and even though the track geometries are quite large, it is possible to see the areas of resin and glass and how they surround the PCB transmission line tracks by closely examining the pair above the upper

maximum copper layer. Figures 3 and 4 show clearly the areas of high glass content and high resin content. With care it is possible to model these areas and make a closer approach to the desired impedance with a minimum number of prototypes.

Figure 1
Approximate field pattern in edge coupled embedded microstrip

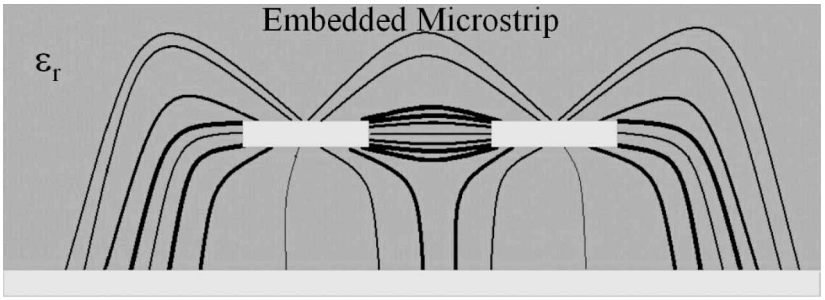


Figure 2
Differential pair in FR4

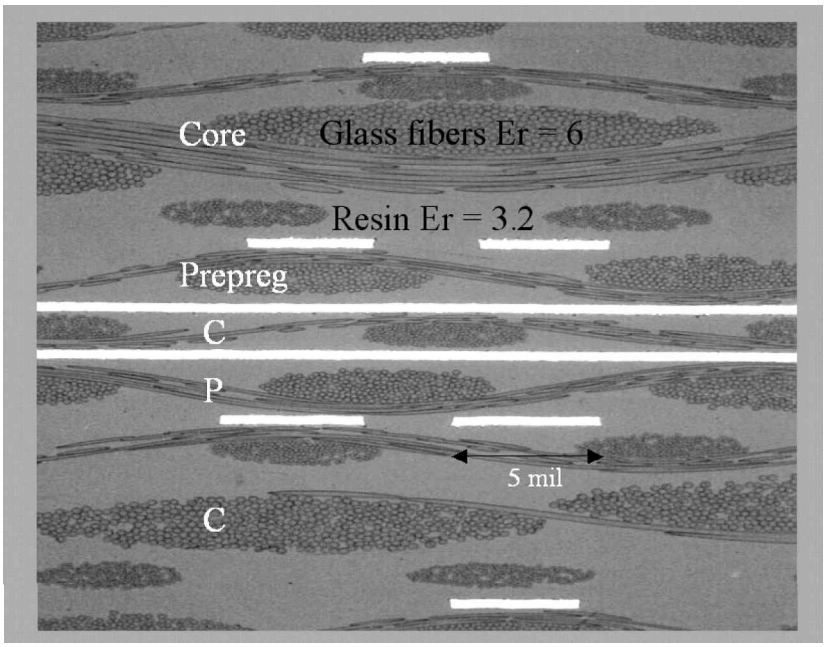
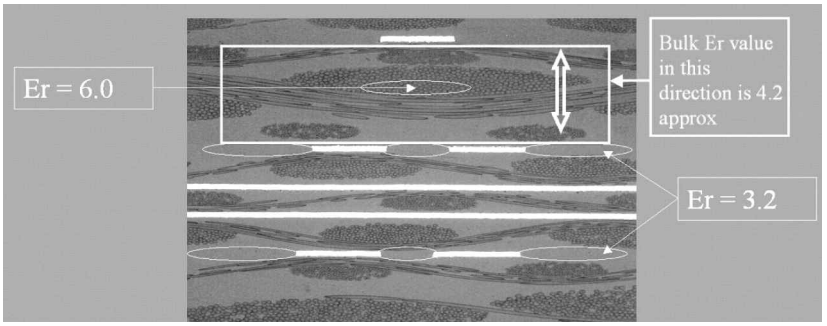


Figure 3



2.4 Polar field solver software Si8000

Polar software uses BEM field solvers. These field solvers model coating and resin rich regions on single and multiple dielectric PCBs. A brief mathematical introduction to the BEM is given in Section 3. A full explanation of the complex mathematical process is beyond the scope of this paper, however the user of the software is able to use this complex modelling through a very simple user interface. The first Polar field solver to employ BEM is called the Si8000, and data are entered and processed either through a desktop calculator style interface called the Quick Solver, or alternatively, the field solvers may be called as embedded Microsoft Excel spread sheets. One particular valuable feature of the Quick Solver Interface (Figure 5) is the ability to enter tolerance values for a range of properties: this enables best and worst case yields to be predicted before production.

In addition, Si8000 recognises the PCB fabricators love of (or battle with) mixed dimensional units. Measurements can be entered in mils (thou), millimetres, inches or microns. The units are then automatically converted to minimise risk of data entry error.

2.5 Modelling of surface traces

It is possible to model the effect of soldermask thickness between differential and coplanar tracks. Impedance changes with changes in solder mask fill can be calculated – shown in Figures 6-8 – as dimension C3. Solder mask thickness between traces is given by C3 (coating between traces) in Si8000 structures.

In this example, Si8000 Quick Solver is used to model the structure with the coatings at minimum and maximum values.

Note the different coating thickness between traces.

Magnified views of the gaps between traces showing different LPI fills are shown in Figure 7.

The Si8000 Quick Solver values and solutions for the structures are shown in Figures 9 and 10.

Using the earlier parameters, an approximately 3 per cent decrease in differential impedance is observed between minimum and maximum coating thicknesses between traces. The impedance change will depend on the separation between the traces.

Graphing the above can give an indication of how production may vary when employing different resist application techniques. This can also be invaluable when prototyping in one facility and producing volume in another. Differences in plant process, which may otherwise be overlooked, could contribute to a yield problem. Here it is possible to pre-empt the effect of process variation and work with front end to consider such differences. Figure 11 shows this with the results of field solving for a range of coating fill depths between a differential pair.

The graph in Figure 11 shows the change in differential impedance against coating thickness between the traces.

Another way of looking at this effect is to consider the field distribution and how it varies with tight and loose coupling.

Figure 12 shows the distribution of electric field in an edge coupled surface microstrip structure. The narrow distribution shows the field in a structure where the differential pair is closely spaced, the broader curves show how the field spreads out as the separation of the traces (S1) is increased. The actual structure is shown underneath and rotated through 90° to help visualise the field distribution.

- The steepest trace shows a strong field between the two traces with no electric field strength at the ground plane.
- Consider the broadest, this represents a differential pair with a larger spacing and the field is distributed all the way down to the ground plane.

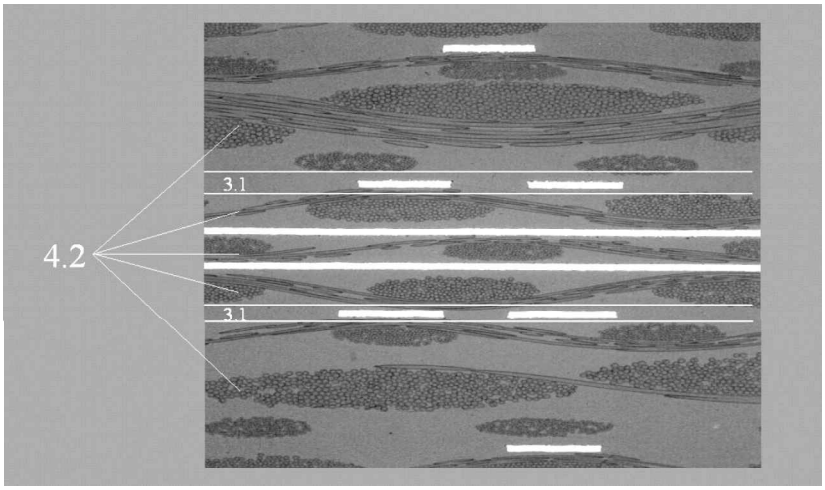
If a glass layer is close to the surface and the traces are closely spaced the field will experience an Er that is closer to glass than resin.

On inner layers the space between the two traces will be filled with resin resulting in a lower effective dielectric constant.

- The amount of variation will depend on the board build and the particular PCB facility and its production process.
- To achieve maximum yields it is necessary to work closely with the PCB manufacturer and consider that PCB laminates do not exhibit "ideal" theoretical behaviour because of their composite nature.

How boundary element numerical techniques are employed to more closely simulate the actual conditions.

Figure 4



3. Brief outline of BEM software

3.1 Introduction to BEM

The BEM is based on the potential (or voltage) V and the voltage gradient $\partial V/\partial n$, on the boundary surrounding a region, where n is the outward normal to boundary. The concept is shown in Figure 13. For our purposes, the voltage gradient is related to the electric field E, through

$$E = -\frac{\partial V}{\partial n}$$

so that E is in the opposite direction to the normal n.

The boundary may have two parts:

(1) the voltage V is known and the electric field E is unknown; and
(2) V is unknown and E is known.

To find the unknown quantities, the boundary is divided into elements, each with a node at each end. Using the interaction between the voltages and the electric field, BEM gives a series of equations between the unknown and known quantities. The solution of these equations means that all voltages and electric fields are known on all boundaries.

The nodes can be distributed non-linearly. The variation of both the unknown values of V and E over an element, has to be assumed. For our purposes the variation is assumed to be linear. This is a compromise between accuracy and convenience, since an integration (numerical) over an element is required, in deriving the coefficients of the equations.

3.2 Mixed dielectrics

As an example, consider the region shown in Figure 13 to be divided into two dielectric regions as shown in Figure 14.

The regions are divided by another boundary. Both the voltages and electric field are unknown on this boundary. However, from the boundary conditions which must apply on this boundary, the voltages as viewed from each region, V_1 and V_2, must be equal and the electric flux densities

Figure 5
Si8000 Quick Solver Interface

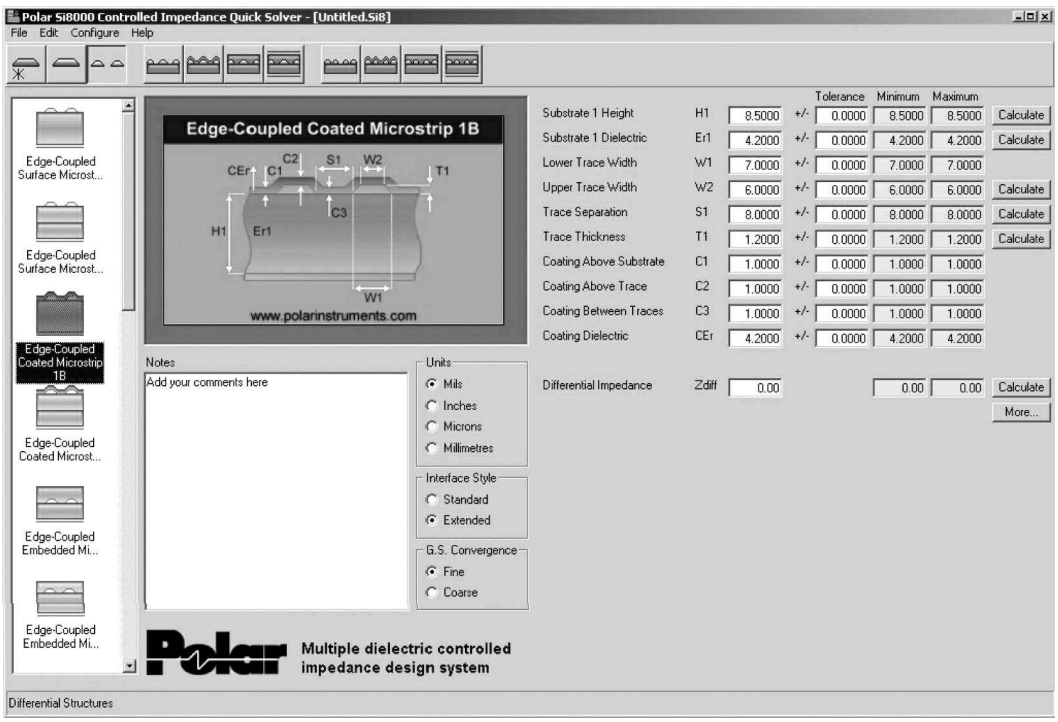


Figure 6
Si8000 model of edge-coupled surface microstrip

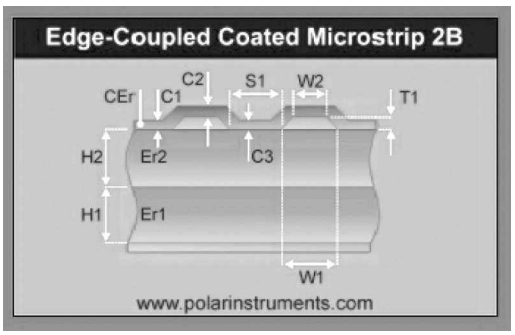


Figure 7
Minimum fill

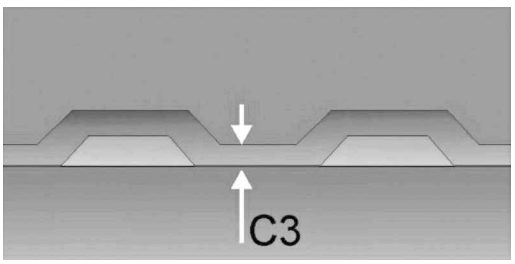
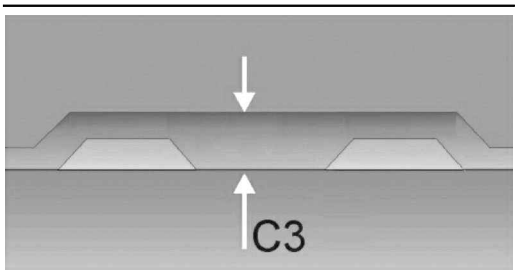


Figure 8
Maximum fill



D_1 and D_2 are continuous, so that,

$$V_1 = V_2$$

$$D_1 = D_2 \quad \text{or} \quad \varepsilon_{r_1}\varepsilon_0 E_1 = \varepsilon_{r_2}\varepsilon_0 E_2$$

Using these conditions and the known conditions on the outer boundary, enough independent equations are obtained to calculate the unknown voltages and electric fields including those on the boundary between the dielectrics.

3.3 Calculation of impedance

The surface of the track is one part of a boundary. The voltage is known and set to 1 V. The ground plane is another part of the boundary and is set to 0 V. On both these boundaries, the electric field is unknown. How the boundary is completed is described later.

The BEM calculates the unknown electric fields and voltages. For our purposes, the E-field on the track is required. From this E-field, the flux density D is obtained using the dielectric constant adjacent to the track surface. The sum of all the flux densities around the track gives the total electric flux Ψ. From Gauss's law, this flux is the charge, Q, on the track. Since the track is at 1 V relative to ground the capacitance is

Figure 9
Minimum mask impedance

Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	1.0000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	85.23

Figure 10
Maximum mask impedance

Substrate 1 Height	H1	4.2500
Substrate 1 Dielectric	Er1	4.2000
Substrate 2 Height	H2	4.2500
Substrate 2 Dielectric	Er2	4.2000
Lower Trace Width	W1	7.0000
Upper Trace Width	W2	6.0000
Trace Separation	S1	3.0000
Trace Thickness	T1	1.2000
Coating Above Substrate	C1	1.0000
Coating Above Trace	C2	1.0000
Coating Between Traces	C3	2.2000
Coating Dielectric	CEr	4.2000
Differential Impedance	Zdiff	82.43

$$C_d = Q_d = \Psi_d$$

The calculation is repeated with all dielectrics replaced by air. This gives the capacitance

$$C_a = Q_a = \Psi_a$$

In air, the velocity of transmission is the velocity of light, $c\,(\approx 3.0 \times 10^8\ \text{m/s})$, so that the inductance is

$$L = \frac{1}{c^2 C_a}$$

from which the impedance is

$$Z_0 = \sqrt{\frac{L}{C_d}} = \frac{1}{c\sqrt{C_d C_a}}$$

Thus, to obtain the impedance, two passes through the BEM calculation are required; one with the dielectric materials present and a second pass without the materials to calculate the inductance.

3.4 Example of boundary configurations

Figure 15 shows the boundary configuration used for a single track surface microstrip with two substrates below the track.

Figure 11

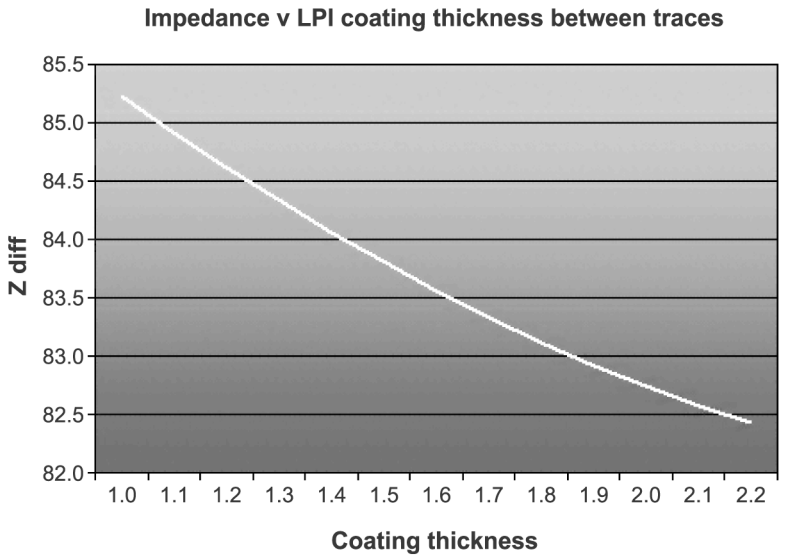
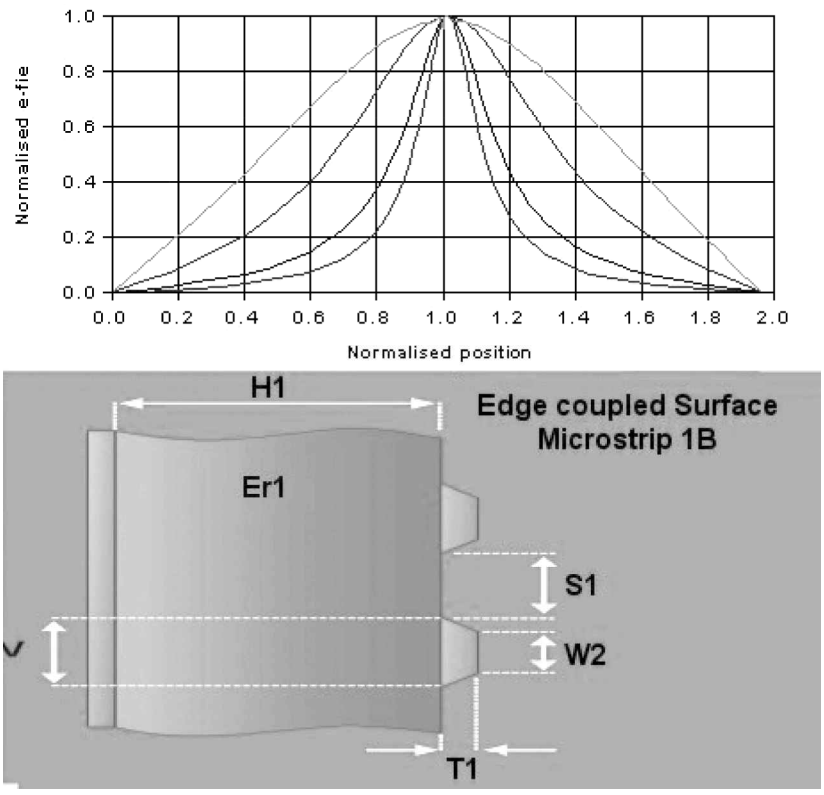


Figure 12
Electric field distribution



Symmetry is used as only half the track is necessary. The substrates are counted upwards from the ground plane. The boundary away from the track is assumed to be at a large distance to represent infinity: the coordinates *xf* and *yf* are large. The boundaries are divided into sections (numbered with arrows in the figure). The direction of these sections is important. Nodes are distributed over these sections and are distributed in a non-linear manner. For instance, at the corners of the track, the electric field is large, so the nodes are very close together. The distance between nodes then increases away from the corners.

The known voltages are on the ground (0 V, sections 16, 20, 17), and the track (1 V, sections 7-9). On the line of symmetry, sections 13, 14, 1, 15, the electric field must be zero. The sections at "infinity" are 18, 4, 10, 11, 12. In principle, the voltage is zero here, but since the boundary is not truly at infinity, better accuracy is obtained by setting the electric field to zero. The voltage on these sections is found to be small, approximately 0.01 V or less. Both the voltage and electric field on the sections forming the boundaries between the regions, sections 5, 6 and 2, 19, 3 are unknown.

Figure 16 shows a differential surface microstrip with a solder mask where allowance has been made for different mask thickness above the track, outside the tracks, and between the tracks. In this example, the line of symmetry is between the tracks: here the voltage must be zero.

3.5 Program layout

Figure 17 shows the basic flow chart of the program.

The *calculate node distribution etc*. phase is a series of functions which take the input data. These functions determine the sections in anticlockwise order for each configuration, determine the start and stop coordinates for each section and finally allocate the non-linear distribution and coordinates for the nodes on each section. Each track configuration is described as a series of bounded regions, and it is possible to cater for a large range of structure possibilities.

The *BEM calculate* phase takes the nodes for each region and calculates the coefficients of the simultaneous (matrix) equations, then solves the matrix for the unknowns and calculates the charge on the track from which the impedance is finally calculated. This phase is the same for all configurations and is unaffected when extra configurations are added.

The output on the screen includes not only the impedance, but also the capacitances, both C_d and C_a, as well as the effective dielectric constant. This last value is needed if the time delay is required. These numeric techniques are very computing intensive, and it is only recently that PC technology has advanced to a point where the field solvers are able to execute in minutes or seconds.

BEM is an ideal technique for multiple dielectric and mixed material builds, lending itself to support a very wide range of structures with the ability to cater for resin rich or glass rich regions, both above and below the transmission line, as well as areas of pure resin between differential and coplanar structures which form during pressing.

4. Finally

Some considerations to ensure that the best data are fedback into the models when learning from a new build and considerations for moving from prototype to volume build.

4.1 Ensure your measurements are valid

Whatever TDR is used to measure impedance, it is important to ensure that it is calibrated to traceable impedance standard. TDR measurements need to be made with the same DC conditions at the end of the trace as those on the TDR head during verification. As most coupons are unterminated, it is good practice to use reference airlines or precision semi-rigid coax which is measured against a traceable standard. Calibrating a TDR with a precision load resistance can introduce measurement errors of up to

Figure 13
Element boundary concept

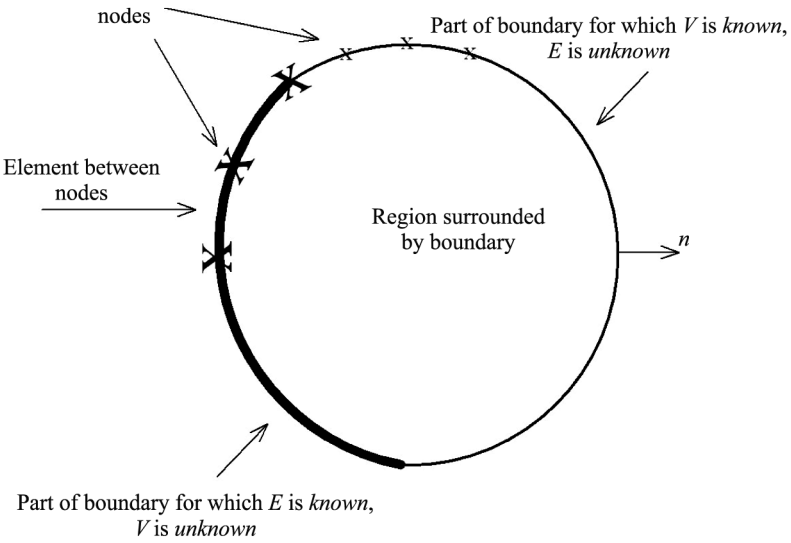
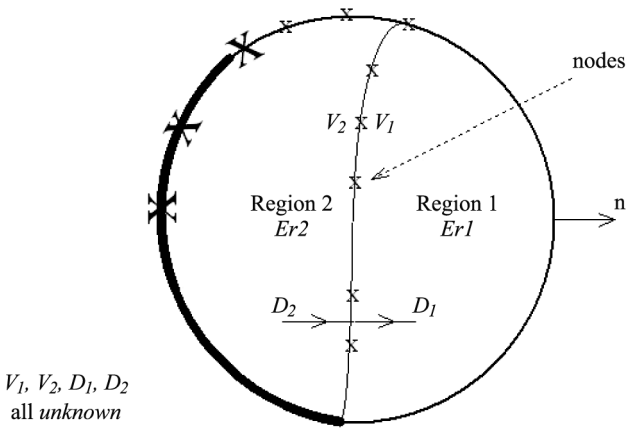


Figure 14
Boundary between dielectrics



3 or 4 Ω at 50 Ω. Laboratory TDRs are typically calibrated for voltage reflection, and it is important to cross check equipment with a known standard to minimise any chance of misunderstanding results. In any study where there is disagreement over impedance results between fabricators/designers/or an OEM, the measurement systems should be compared against a traceable standard. IPC 2141 (replaces D 317) and the soon to be released revision of IPC TM 650 clearly call out the use of air lines as standards for calibration and verification of impedance test systems.

4.2 Discussion forums, independent advice and other resources

Whenever working in high speed domains often it is helpful to ask for some third party advice. Occasionally, there may be some misunderstanding between an OEM and a fabricator over board measurements. Polar is always pleased to assist, but would also recommend to seek advice from the e-mail forums such as IPC Designer Council, TechNet, or Si-List (for signal integrity discussions). When trying to track down the source of variation between prediction and measurement, it may often be necessary to microsection to obtain the true source of discrepancy. Ideally, test coupons should be employed for measurement as, if a discrepancy is proved to be a measurement error on the part of the inward inspection, one has only sectioned a coupon, and not the board itself. Polar maintains a comprehensive resource section at www.polarinstruments.com. Polarinstruments.com aims to provide a resource of helpful technical information aimed at fabricators who are new to high speed analog or digital PCB fabrication. The site is constantly updated with answers to high speed questions as they are solved.

4.3 Some background on achieving maximum yields

The best PCB fabricators take statistical data from impedance test and feed it back into the production process. Often these data suggest that nominal line widths may need to be altered from the original design. This is a surprise to many PCB designers who are accustomed to submitting Gerber to the PCB manufacturer who then turns the data into finished boards without adjustment. High-end CAD systems sometimes calculate line widths assuming homogeneous perfect materials; often, these tools give an “ideal-world” calculation of line width. Real PCBs will differ depending

Figure 15
Surface microstrip: two substrates

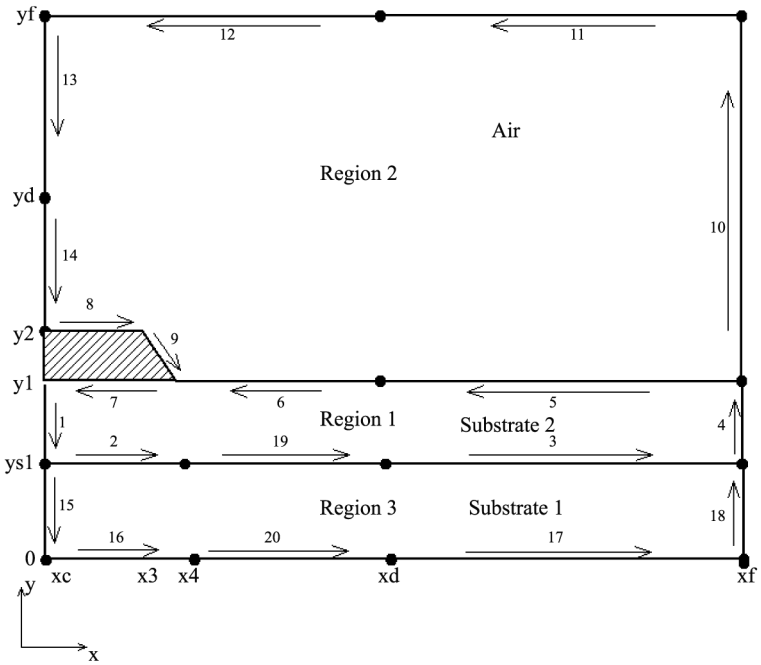
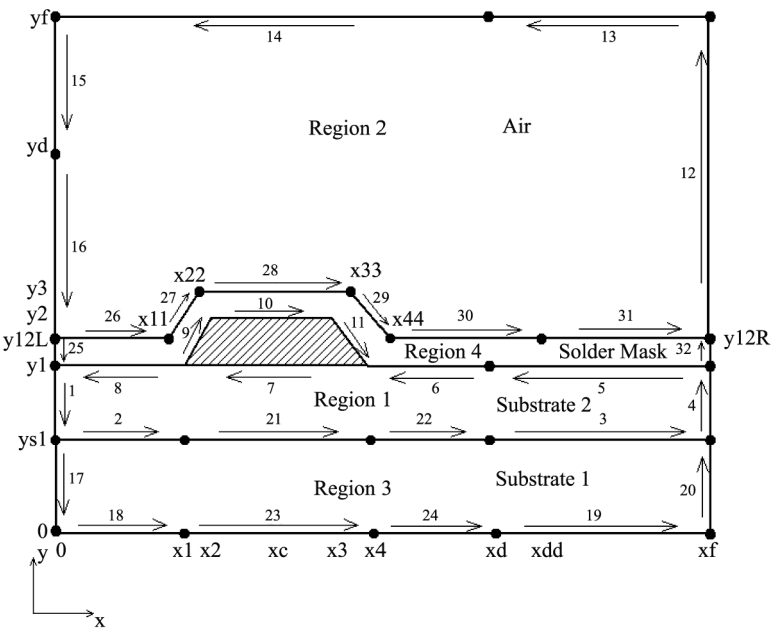


Figure 16
Surface differential: two substrates and solder mask

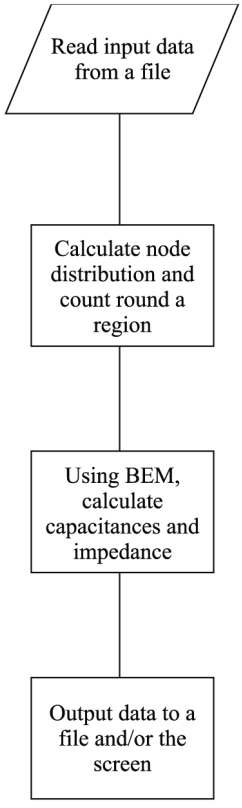


on the source of prepreg and core materials, the glass resin ratio after pressing, and the etched trace geometry. Ideally, one should identify controlled impedance trace widths separately from other traces of the same nominal width. Impedance design systems such as the new Polar Si8000m allow us to model one step closer to real world processes by employing boundary element method field solvers capable of setting Er on a layer by layer basis, and allowing for compensation of resin rich areas between tracks www.polarinstruments.com/support/cits/AP148.pdf.
If possible, allow front-end engineers to alter the nominal dimensions (within acceptable limits) in order to achieve maximum yields.

4.4 Prototypes and volume production

With the huge structural changes taking place in the board fabrication industry, and the ease of moving manufacturing data from one region to another, it is easy to overlook some of the variations between plant, chemistry and laminate styles that can occur from region to region. If one supplier builds a prototype run in one country and the volume

Figure 17
Basic program flow chart



product is produced by an associate fabricator in another region then it is quite possible that the boards will have different characteristics from a high speed signal integrity point of view. Considering the above point when moving from prototype to volume build, multiple dielectric modelling software allows the effect of substituting locally sourced materials and processes to be predicted. For example, the soldermask process may differ and by modelling coating thickness adjacent to and between high speed traces, adjustments may be made to the data to compensate for any variation. When making adjustments at front end or in the process it is essential that a good dialog is maintained between fabricator and original design authority. The authors continue to be surprised at how often electrical designers are unfamiliar with the PCB production process. Educating new electrical designers and experienced electrical designers who are still unfamiliar with fabrication is a constant challenge for both fabricators and their suppliers. Often, a fabricator is given a complex build by a third party and is unable to ask for more information from the original designers. This is a situation that needs to be improved as boards become more complex and behave more as complex components in their own right.

5. Conclusion

Modelling the characteristic impedance of PCB substrates is a mix of art and science, mathematical tools are available to assist in this process but, as in all mathematical modelling processes, the input data must be good if the model is to achieve the highest accuracy. Applying knowledge of the electrical properties of the constituent components of the substrate materials to obtain a best estimate of the local dielectric constant of a structure will ensure that the modelling software makes the closest prediction of the finished transmission line characteristics. It is always necessary to ensure that one examines the process as a whole and there is confidence that the measurement system is also providing traceable measurements to enable the design/model/prototype/fabricate loop to be closed.

Reference

Alan Staniforth, J. and Gaudion, M. (n.d.), "The effect of etch taper, prepreg and resin flow on the value of differential impedance", *Presented at IPC Expo 2002.*