Practical Papers, Articles and Application Notes

Robert G. Olsen, Technical Editor

In this issue you will find three practical papers that should be of interest to members of the EMC community. The first is entitled "PDN Design Strategies: I. Ceramic SMT Decoupling Capacitors – What Values Should I Choose?" by James L. Knighten, Bruce Archambeault, Jun Fan, Giuseppe Selli, Samuel Connor, and James L. Drewniak. These are the people you would like to hear discuss this topic and since this is the first in a series of papers they plan to write, we will hear from them again. There is little need to provide extra motivation for the topic since as the speed of digital systems goes higher, the subject of power supply decoupling will become even more relevant than it is now. The second paper is entitled, "Wireless Phone Threat Assessment for Aircraft Communication and Navigation Radios" by T. X. Nguyen, S. V. Koppen, L. J. Smith, R.A. Williams and M. T. Salud. This is a subject that those of us in EMC think about nearly every time a flight attendant tells us to turn off digital devices when we are about to take off. Commissioned by the FAA, this well written piece of work is a thorough discussion of out-of-band emissions. The third paper is entitled, "TEM Cells for Whole Aircraft EMV Testing" by Andrew J. Walters and Chris Leat. In this paper the authors show how a combination of theoretical and experimental techniques can be used to optimize the performance of TEM cells for electromagnetic vulnerability studies of full sized aircraft. The latter two papers were first presented at the 2005 IEEE International Symposium on EMC in Chicago and have been reprinted here by permission of the Symposium Committee.

The purpose of this section is to disseminate practical information to the EMC community. In some cases the material is entirely original. In others, the material is not new but has been made either more understandable or accessible to the community. In others, the material has been previously presented at a conference but has been deemed especially worthy of wider dissemination. Readers wishing to share such information with colleagues in the EMC community are encouraged to submit papers or application notes for this section of the Newsletter. See page 3 for my e-mail, FAX and real mail address. While all material will be reviewed prior to acceptance, the criteria are different from those of Transactions papers. Specifically, while it is not necessary that the paper be archival, it is necessary that the paper be useful and of interest to readers of the Newsletter.

Comments from readers concerning these papers are welcome, either as a letter (or e-mail) to the Technical Editor or directly to the authors.

PDN Design Strategies: I. Ceramic SMT Decoupling Capacitors – What Values Should I Choose?

James L. Knighten [1], Bruce Archambeault [2], Jun Fan[1], Giuseppe Selli[3], Samuel Connor[2],

and James L. Drewniak[3]

I. INTRODUCTION

This article is the first in a series of articles on strategies for the design of dc power distribution networks (PDN) on modern digital printed circuit boards (PCB). In high-speed digital circuit designs, the PDN associated with the PCB plays a vital role in maintaining signal integrity (SI), i.e., necessary fidelity of signal and clock wave shapes, and minimizing electromagnetic noise generation. Yet, the design of the power distribution system presents an increasingly difficult challenge for digital circuits employing active devices. As integrated circuit (IC) technology is scaled downward to yield smaller and faster transistors, the power supply voltage must decrease. As clock rates rise and more functions are integrated into microprocessors and application specific integrated circuits (ASICs), the power con-

sumed must increase, meaning that current levels, i.e., the movement of electrical charge, must also increase [1-2].

One category of design engineer who confronts this design challenge is the signal integrity (SI) engineer, whose goal is to ensure adequate fidelity of the individual signal and clock wave-shapes on the PCB [2-4]. Another category of engineer who faces similar design challenges is the electromagnetic interference/compatibility (EMI/EMC) engineer, whose goal is to minimize electrical noise generated by the circuitry to prevent interference with other systems and within the same system [5-8]. While both engineers wrestle with the same physics of the dc PDN on a digital PCB, practitioners of different design disciplines may view the same physical phenomena differently. For instance, the SI engineer may be more familiar with circuit behavior and analysis expressed

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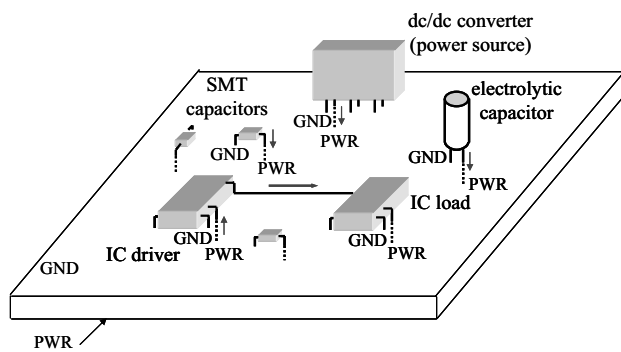3 University of Missouri-Rolla, MO, gs5xd@umr.edu and drewniak@umr.edu

Figure 1: A power bus (power and ground plane pair) on a typical digital PCB is populated with active IC devices along with power delivery devices such as dc-dc converters (VRMs) and capacitors of various types.
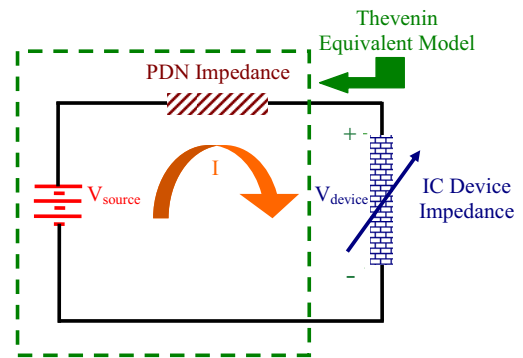

Figure 2: A digital IC is powered by a PDN. Changes between low and high states cause a changing current demand from the IC which causes the dc voltage across the IC to fluctuate. This voltage fluctuation is inevitable and represents an ac voltage ripple on the dc voltage level which is a source of ac noise on the PDN.

in the time domain than with the behavior of electromagnetic waves and analysis expressed in the frequency domain. The EMI engineer's experience is likely just the reverse. Therefore, these engineers may employ different methodologies and approaches to PCB design. These different design methodologies may sometimes seem contradictory and/or incompatible, but both engineers have similar goals of assuring adequate charge transfer between active devices and the PDN with minimum noise generation. This series of articles is intended to review the state of knowledge of dc power distribution design, offer practical design advice, and address schools of design that appear to offer conflicting advice.

The PDN for modern medium-to-high-speed digital PCBs is usually formed from one or more pair of conducting planes used as power and ground (power return). The PDN for digital circuitry has evolved over time, as signal and clock speeds have increased, from discrete power supply wires, to discrete traces, to area fills and ground islands on single/two-layer slow-speed boards, to the planar power bus structure used extensively in today's multi-layer high-speed PCBs. The low inductance associated with charge delivery from the plane to circuit element allows for the storage of relatively easy-to-deliver charge available all over the board. Often the term power bus is used to identify an individual plane pair, whereas the term PDN is used for the entire system of supplying power to circuits placed on the PCB. Figure 1 illustrates a typical power bus populated with an assortment of devices often found on digital PCBs, i.e. dc-dc converters, ICs, and capacitors. As speeds of active devices have increased, digital data rates have escalated and signal rise and fall times dropped so that the frequency regime of operation on the PCB has risen into the gigahertz (GHz) band. Operation at high frequencies can blur the boundaries between circuit behavior and electromagnetic behavior.

Noise is generated in the power bus when a digital active device (integrated circuit or transistor) switches between high and low logical states (switching noise) [5], or it can be coupled to the power bus when a high-speed signal transits through the power bus by signal vias (transition noise) [9,10]. Noise generated in the power bus can be easily propagated throughout the board. Propagated noise can affect the operation of other active devices (signal integrity) as well as radiate from the PCB (EMI). At the printed circuit board (PCB) level, there is no way to

eliminate the production of noise by IC devices. However, a good PCB design can ensure that the generated noise be constrained to a level that permits successful circuit operation and the resulting low levels of radiation produced do not violate regulatory requirements. The use of decoupling capacitors is one of the key elements in achieving this goal, along with the board stack up design, power/ground plane pair, usage of losses, power islands, board edge termination, etc.

II. THE POWER BUS FUNCTION

There are two primary purposes of the PDN. The first purpose of the PDN is functionality. The PDN is a charge storage and delivery system that supplies charge (current) when an IC switches state and requires additional current. As seen in Figure 2, the voltage at the device varies with current drawn from the PDN because the PDN impedance is non-zero. The lower the value of the PDN impedance, the lower its effect on the device voltage will be. If sufficient current is not provided, the IC may experience a functional failure. The voltage (V_{device}) at the IC power pin fluctuates with charge demand so as to manifest an AC voltage ripple that is added to the dc level. The magnitude of this ripple is related the magnitude of the current and the PDN impedance, which is discussed in succeeding sections.

A second purpose of the PDN is to reduce or minimize the noise injected into the power and ground-reference plane pair and thus reduce the potential of noise propagation in the board and EMI emissions from the circuit board. The mechanisms for EMI emissions are several. For instance, the edge of a board may be near the seams of a metal enclosure or near an air vent area, allowing this noise to escape the enclosure. Alternatively, PDN noise may couple onto input/output (I/O) connector pins or onto a grounded cable shield and be directly coupled out of the metal enclosure through any of the cables. There are a variety of coupling mechanisms that are possible once this noise is created. To avoid undesirable consequences from noise on the PDN, the impedance of the PDN should be low over a wide frequency range that includes the spectrum of the critical signals and their harmonics.
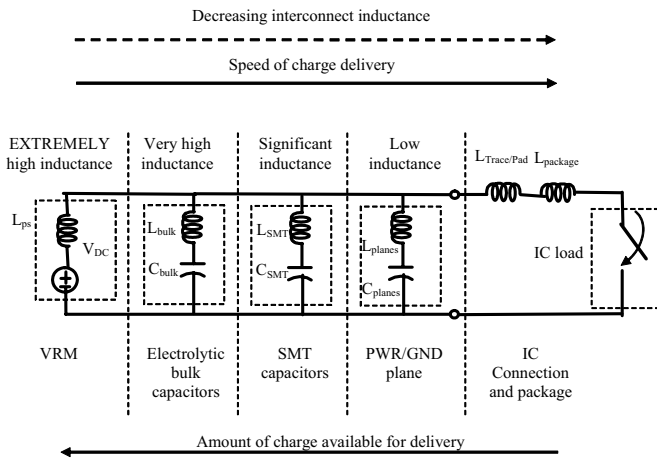
Figure 3: A hierarchal design of capacitive decoupling provides both the needed quantity of available charge and the required rapidity of delivery.

III. THE DECOUPLING CAPACITOR

A PDN is comprised of several elements, including the VRM module, bulk capacitors, SMT decoupling capacitors, and power/ground plane pairs (power bus). The effectiveness of each element in delivering sufficient charge with adequate speed is not uniform. A charging hierarchy, as seen in Figure 3, exists based on the rate of charge delivery (usually impeded by distance and inductance) and charge storage capacity [2].

The VRM (Voltage Regulator Module, i.e., dc/dc converter), the largest source of charge, is able to store and release a lot of charge but it cannot meet demands to rapidly deliver charge due to the large inductance connecting it to the PDN. It cannot keep up with charge demands that vary or oscillate with rapidity greater than a MHz. Hence, it cannot deliver charge in a timely manner when the circuits demanding charge have time constants that are much shorter than one microsecond.

Bulk capacitors constitute the second largest source of charges in this hierarchy and are typically capacitors whose values range between a few hundred microFarads to as high as a few milliFarads. These components are able to supply charge with sufficient speed to meet the demands by systems characterized by time constants as low as a few hundreds of nanoseconds and even shorter.

Decoupling capacitors, sometimes referred to as "high-frequency ceramic capacitors", are the second to last category of components in this charging hierarchy [2]. Decoupling capacitors usually exhibit capacitance values from a few tens of nanoFarads to as high as a few microfarads. These capacitors can usually support charge demand from circuits with time constants as low as a few tens of nanoseconds.

The PWR/GND planes form the last component in the charging hierarchy and can usually deliver charge to circuits whose time constants are shorter than a few tens of nanoseconds, i.e., a charge demand frequency above several hundreds of MHz.

The VRM and the bulk capacitors are usually few in number and are located in specific areas of the PDN due to their dimensions and other constraints. High-frequency decoupling capacitors are usually large in number and are typically easily located with a greater flexibility. A subsequent article will address where to place high-frequency capacitors for effective decoupling. Figure 4 shows a typical impedance profile of a decou-
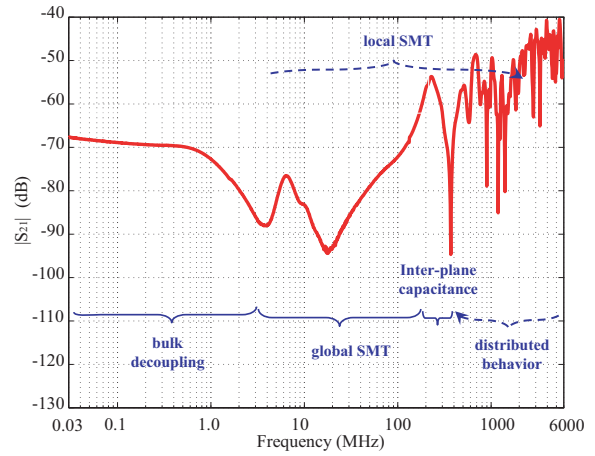

Figure 4: An S_{21} profile of a decoupled PDN shows typical ranges of effectiveness of contributors to the hierarchal decoupling strategy. S_{21} is related to the transfer impedance between two points on a PDN. Much of this article refers to "Global" SMT decoupling. Local SMT refers to location dependant decoupling that is discussed in future articles.

pled PDN.

Impedance plots (driving point, or , and transfer impedance, or) versus frequency are often used to evaluate the behavior of a power bus. In general, is defined as

(1)

where = the voltage at a location on the power bus, labeled, port i

and, = the current at a location on the power bus, labeled, port j, and all other ports are open circuited, i.e., for

Therefore, provides an indication of the voltage created by the injection of noise current. indicates the noise transmission from noise source to anywhere on the board. is very useful for circuit susceptibility and radiated emission studies. is a vector quantity in that it has both magnitude and phase. For these types of studies, often just the magnitude is examined.

Interconnect Inductance

The decoupling capacitor exhibits parasitic inductance and resistance in addition to its capacitance. The parasitic inductance consists of an inductance associated with the capacitor itself (equivalent series inductance, or ESL) and inductance associated with the means of connecting the capacitor between power and ground planes (inductances associated with the solder pads used to secure the capacitor to the PCB and any traces and/or vias used to make the electrical connections). This is illustrated in Figure 3 as L_{SMT} for high-frequency SMT capacitors and L_{BULK} for bulk capacitors. The parasitic inductance impedes changes in the current; hence, it impedes the prompt availability of charge. The parasitic inductance and resistance when combined with the device's capacitance form a series resonant circuit whose impedance dips to a minimum at the frequency where the inductive and capacitive reactances cancel, as shown in Figure 5. At frequencies higher than this resonant frequency, the capacitor behaves inductively and is ineffective in decoupling. [2, 5]
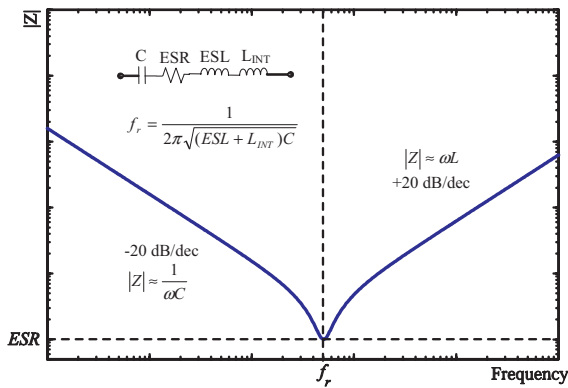
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Figure 5: Parasitic elements of the capacitor (resistance and inductance), along with inductance of the traces, pads and vias that connect the capacitor to the planes form a series resonant circuit that exhibits an impedance minimum at the frequency where the reactances cancel. Lowering inductance moves this resonance higher in frequency, causing the capacitor to function as a capacitor at higher frequencies, demonstrating why inductance from traces, pads, and vias can be detrimental to effective decoupling.

If the resonant frequency is shifted higher in frequency by lowering the parasitic inductance, decoupling can be made more effective at higher frequencies. Since the capacitance is fixed as the value of the component, design attention is usually paid to the inductance associated with the capacitor and its interconnect. Low values in interconnect inductance can often be achieved by careful attention to the design of solder pads lands with low inductance properties along with having no traces in the ideal case, or in the realistic case, very short traces connecting them to the planes [4]. The design of the land patterns for the decoupling capacitors has evolved during the years [2]. The parasitic inductance of the interconnects has been lowered from several nH to less than 1 nH. In brief, a good PDN design is characterized by a low interconnect inductance between each decoupling capacitor and the PDN itself. Figure 6 illustrates the connection of an SMT capacitor to a power bus which provides a parasitic inductive component from the current path above the plane (Loop 2) and a parasitic inductive component associated with current flow between the planes, first in the via and then returning as displacement current (Loop 1). As stated earlier, the parasitic inductance associated with current flow above the plane also includes effects from the solder pads that connect to the capacitor and any traces used to connect solder pads to the vias.

The decoupling capacitor's capacitance along with the overall parasitic inductance and its ESR forms a resonant RLC circuit, whose time constant or envelope is proportional to the overall parasitic inductance. The time constant of a series RLC resonant circuit is given by

$$2L/R \qquad (2)$$

The lower the value of the inductance, the faster the capacitor can supply and store charge and the more importance that is attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior.

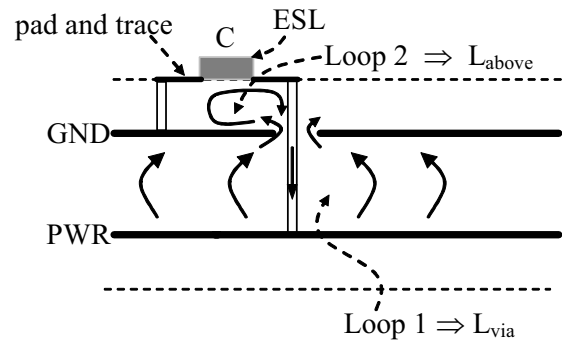The ESL of the decoupling capacitors is a function of the

Figure 6: The connection of an SMT decoupling capacitor to the surface of a PCB produces parasitic inductance associated with current flow in the loop above the plane and parasitic inductance due to current flow between the planes.

length, width and height of the capacitor itself. Due to improvements in the material selection and manufactory technology, the size of SMT decoupling capacitors have been shrunk from the early 1206 package size (120 mils length x 60 mils width) down to the more recent 0201 (20 mils length x 10 mils width) package size, allowing a significant reduction of the equivalent series inductance, which is always less than 1 nH.

The equivalent series inductance (ESL) as well as the equivalent series resistance (ESR) are usually measured by employing impedance analyzers and/or network analyzers. In both cases, special fixtures are utilized along with calibration procedures and measurement techniques in order to minimize the parasitic elements associated with the measurement setup itself [11]. Values reported by capacitor manufacturers are influenced by the specific measurement techniques employed and should be viewed critically when the use of the specific values of parasitic elements is desired.

A very large selection of decoupling capacitors is available to designers. Given the wide range of package sizes, materials (Electrolytic, Tantalum or Ceramic X7R, X5R, Y5V, etc.) and manufactory technologies (MLC, LLIC, IDC or LICA), a good PDN design might be carried out in various ways. Ceramic capacitors are characterized by lower ESL than electrolytic and tantalum capacitors, even if the latter are usually available in the same package size. In fact, the multilayer configuration of the ceramic capacitors (MLC) allows controlling the values of the equivalent series inductance by adjusting the height, width, length and number of pad connections, accordingly [2]. Several fabrication technologies are available for ceramic capacitors, i.e., the reverse geometry or low inductance chip capacitor (LLIC) configurations, where the current flows into the decoupling capacitor from the wide sides, the interdigitated configuration (IDC), where multiple connections are employed, and the low inductance chip array (LICA) configuration, where the decoupling capacitor is mounted as a flip-chip component [12].

Determining Individual Decoupling Capacitor Values – Differing Approaches
Approach A: The SI community
Two general approaches have developed in the design community on how to deploy decoupling (high-frequency ceramic) capacitors in order to reduce the impedance of the PDN between frequencies in the range of approximately 1 MHz to a
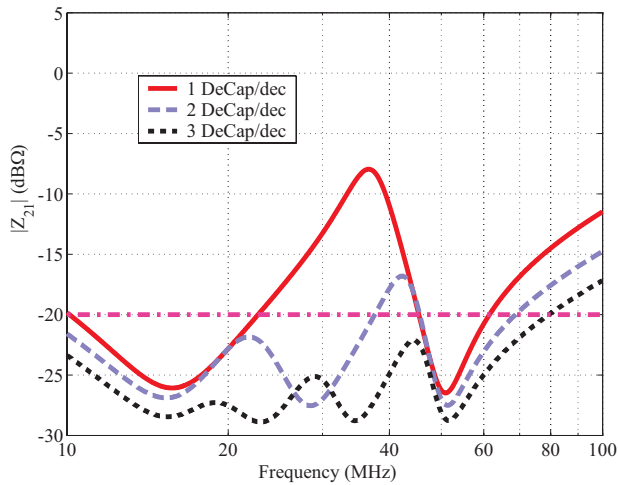
Figure 7: Approach A is shown with three different densities of capacitor values. Three capacitor values per decade is a commonly used array density which produces an impedance profile that is reasonably flat.

few hundred MHz. A prominent approach, referred to here as Approach A, is used in the SI community and has developed out of the experience of server motherboard design and other high performance digital PCBs [2-3]. This approach uses an array of values of decoupling capacitors. This technique generally uses three capacitor values per decade to achieve the flattest PDN impedance vs. frequency profile to maintain an upper bound "target impedance" to provide an upper bound on the AC ripple voltage on the PDN [4, 13].

In Approach A, the capacitor values are typically chosen so that they are logarithmically spaced (i.e. 10, 22, 47, 100 nF, etc). The effectiveness of this approach is somewhat dependant
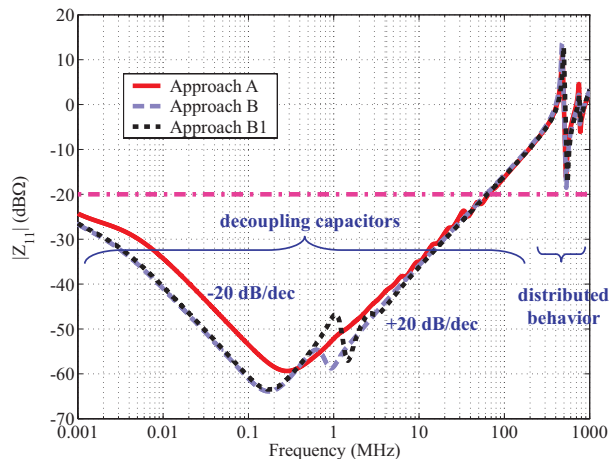

Figure 8: The driving point impedance, Z_{11}, of a power bus showing a comparison of design Approaches A and B for choosing the values of individual decoupling capacitors in the frequency range from 1 kHz to 1 GHz. Both approaches meet the desired target impedance requirements in the frequency range of interest. The impedance in Approaches B and B1 reach an initial minimum at a lower frequency than Approach A because the overall capacitance in these approaches is higher. The impedance minimum for Approach A is not as low as the minimum for the other approaches because the net ESR of the capacitors in Approach A is higher than the net ESR in either Approach B or B1.

Capacitor Description					# of Caps		
Value (nF)	ESR (mΩ)	ESL (nH)	Inter-connect (nH)	Type	A	B	B1
3.30E+06	60	15	2	E-lytic	1	1	1
100000	11	1.4	2	1812	4	16	16
47000	12	1.4	2	1812	4		
22000	14	1.4	2	1812	4		
10000	16	1.4	2	1812	4		
4700	16	0.5	1.6	0603	4	24	
2200	19	0.5	1.6	0603	4		
1000	23	0.5	1.6	0603	4		
470	29	0.5	1.6	0603	4		
220	23	0.5	1.6	0603	4		
100	30	0.5	1.6	0603	4		
47	40	0.4	1.35	0402	4	20	44
22	55	0.4	1.35	0402	4		
10	75	0.4	1.35	0402	4		
4.7	104	0.4	1.35	0402	4		
2.2	211	0.4	1.35	0402	4		
Total # of Decoupling Capacitors =					61	61	61
Total Capacitance (milliF) =					4.05	5.01	4.90

Table 1: The details of the numbers of capacitors and their values used in the simulation comparisons of Approaches A, B, and B1.

on the value of ESR of the capacitors and the resulting series/parallel resonant (resonant/anti-resonant) frequencies of the decoupling capacitors to maintain the impedance to be below the desired target impedance over the frequency range of interest.

The use of two capacitor values (i.e. 10, 33, 100 nF, etc) or a single capacitor value (i.e. 10, 100, 1000 nF, etc) per decade can be employed but does not usually provide a PDN impedance profile that is sufficiently flat [4]. An example of Approach A with differing densities of arrays of capacitance values is shown in Figure 7. The target impedance is chosen to be -20dBΩ (0.10 Ω) between 10 MHz and 100 MHz. Three different decoupling capacitor arrays are considered: a three capacitor/decade array of 100nF, 47nF, 22nF and 10nF; a two capacitor/decade array of 100nF, 33nF and 10nF; and a single capacitor/decade array of 10nF and 100nF. A series inductance of 1nH and resistance of 50 mΩ are considered in series with each capacitor. The target impedance is exceeded at some frequencies due to the parallel resonances.

Approach B: The EMI community

On the other hand, a prominent view in the EMI community for PDN design for high-speed digital PCBs is that the specific values of decoupling capacitors need not be as carefully chosen as in the previous approach [5]. This design methodology, Approach B, addresses the high-frequency ceramic decoupling specifically and employs the largest value of capacitance available in the specific surface mount technology (SMT) package size to yield a PDN impedance profile that is acceptably flat. For the same number of high-frequency ceramic decoupling capacitors, more total capacitance is often achieved in Approach B than with Approach A.

A comparison of the two approaches in the frequency range between 1 kHz and 1 GHz using a 2-D cavity model method, allowing parallel plane characteristics to be included, is shown

in Figure 8 [14, 15]. The PDN dimensions correspond to a PCB that is 6 in. x 9 in. with a single power/ground plane pair power bus of thickness 10 mils. The PCB material is chosen to exhibit a dielectric constant of 4.5, and a loss tangent of 0.02; a relative permeability of unity; and a plane capacitance of 2.426 nF. For each example with this PCB, one bulk decoupling capacitor and 60 ceramic decoupling capacitors were chosen. In addition, it was assumed that the power bus was located at the center of the 62 mil PCB stackup and that all decoupling capacitors were placed on the board's surface, allowing for inclusion of the via interconnect inductance in the simulation. As shown in Figure 7, a target impedance of -20 dBΩ was chosen. Table 1 shows the specific values of capacitors chosen. For each capacitor type, typical values of ESR and ESL were selected from typical values from a specific vendor's catalog for X7R MLC capacitors. [16]

A third approach, Approach B1, a subset of Approach B, was included to investigate the effects of making all of the smaller decoupling capacitors in the 0402 package size, instead of dividing them between the 0603 (60 x 30 mils) and the 0402 (40 x 20 mils) package sizes. Figure 8 shows the driving point impedance, ‖ of the PDN and Figure 9 shows the transfer impedance, ‖. While there are differences between the three approaches shown in the Figures, all three provide an impedance well below the target impedance up to frequencies in the range of 100 MHz. At low frequencies, Approaches B and B1 provide a lower impedance, which is a manifestation of the higher capacitance used. It is also interesting to note that there is very little difference between Approaches B and B1, except near 1 MHz, where the impedance is already very low compared to the target impedance. Above a few MHz, when the impedance rises proportional to frequency, i.e., at a rate of 20 dB/decade, there is virtually no difference between any of the methods. In this example, above 100 MHz, the discrete decoupling capacitors do not do a good job of maintaining a low PDN impedance, regardless of the design strategy.

In these examples, it is clear that either approach can achieve the design goal on PDN transfer impedance and have nearly identical performance above frequencies of a few hundred MHz. Use of a single value of capacitance in the largest value in the package size may provide the benefit of simplicity of design and manufacture [7]. Changing the design parameters (PCB characteristics, power bus characteristics, capacitor characteristics, etc.) will alter the impedance curves regardless of the design approach used, but will not change the overall conclusion that there is little difference in the PDN impedance profiles between Approaches A and B (and B1).

Although the values of the decoupling capacitors employed are different in the two strategies, the need of lowering the parasitic inductance associated with the decoupling capacitors is consistent [2,3,5,8]. In fact, lowering this inductance shifts all the series/parallel resonant frequencies higher and in particular the last one, allowing the PDN to meet the design specifications on the target impedance in a broader frequency band.

IV. CONCLUSIONS

A low-noise PDN on a digital PCB is important in reducing EMI emissions and in providing supply voltages to ICs that are sufficiently noise-free to prevent data errors. Decoupling capacitors are usually placed between the power and ground-refer-
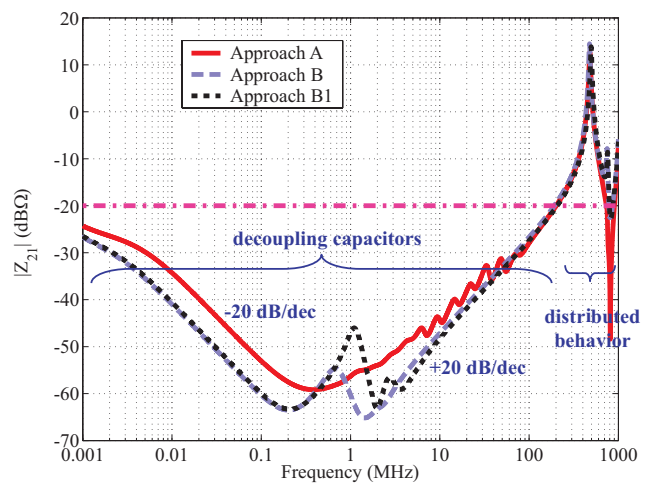

Figure 9: The transfer impedance magnitude, Z_{21}, between two points on a power bus showing a comparison of design Approaches A and B for choosing the values of individual decoupling capacitors in the frequency range from 1 kHz to 1 GHz. Both design approaches meet the desired target impedance requirements in the frequency range of interest.

ence planes to help maintain this voltage. There are two main purposes for decoupling capacitors; (1) provide sufficient charge/current to the IC as it switches states and, (2) reduce noise between the planes which may result in noise propagation and EMI emissions.

The overall decoupling strategy usually employs a hierarchy of decoupling capacitors. Large capacitors (bulk) are used to supply a high volume charge/current storage reservoir, but deliver the current slowly due to the relatively high inductance associated with the capacitor and its circuit. Smaller capacitors usually have less inductance, therefore they can provide current faster. Charge can be provided even faster from the stored charge between the planes in the vicinity of the IC. (Decoupling capacitors in the IC package or on the actual die itself provide the fastest charge.) Typically, the capacitors that deliver charge the fastest are the smallest capacitors, although they have limited amounts of charge they can deliver. Hence, the hierarchical design of decoupling provides some capacitors that yield a limited amount of charge very quickly, and others deliver more charge, but more slowly.

The overall limiting factor of the speed of charge delivery is inductance. Inductance is dominated by the current loop area. Therefore, the spacing between the vias connecting the capacitors to the planes, the spacing between the planes, the distance between the capacitor and the IC influence the inductance associated with the decoupling capacitor. Often, the only impact a physical designer of a PCB can have is to keep the connection inductance of the capacitors as small as possible. This means keeping the vias that connect the capacitor and the planes close to the capacitor body (avoid traces between pad and via) and to use solder pads that minimize the interconnect inductance.

This article compares the effectiveness of two common design approaches for maintaining a PDN impedance below a desired target impedance over a wide frequency range. Approach A, often used in the signal integrity design community relies on an array of decoupling capacitor values (the preva-

lent array being a logarithmic array of three capacitor values per decade of value). Approach B, more prevalent in the EMI design community, is less structured but teaches that use of the largest capacitor value in a package size is sufficient for meeting a low target impedance requirement. Simulations demonstrate that either approach can be effective in maintaining a low target impedance. Designers using Approach A often regard capacitor ESR as an important factor in managing the amplitudes of the alternating resonances and anti-resonances that the array of capacitor values produce. Designers using Approach B are often less concerned with ESR. A primary benefit of Approach B is its simplicity. Decisions on which approach is better for a particular design should depend on design factors other than the ability to maintain a low PDN impedance since both approaches can be effective.

General design implications may be drawn based on this discussion of the methods of properly choosing high-frequency ceramic decoupling capacitor values in a modern digital PCB. Design Implications:

- Decoupling capacitors serve two purposes:
  – Help meet demands for charge by switching ICs
  – Reduce noise in power/ground-reference planes
- Design for a low PDN impedance for good signal and EMI behavior.
- Use a hierarchical array of capacitors to satisfy charge delivery demands. Large (bulk) capacitors provide large amounts of charge slowly. Small capacitors provide lesser amounts of charge rapidly.
- Inductance of the decoupling capacitor circuit determines its effectiveness. ESL, current path loop area, and interconnect detail determine this inductance.
  – Avoid the use of traces to connect solder pad to via
  – Use low-inductance solder pads for SMT decoupling capacitors
  – Low ESL capacitors may enhance decoupling effectiveness at high frequencies
- Either a logarithmic array of ceramic decoupling capacitor values, or just a few values (largest value in a package size) can keep the PDN impedance satisfactorily low over a wide frequency range.

This article is the first in a series of articles on decoupling a digital PCB power distribution network. The next article in this series will address high-frequency capacitor location, i.e., (a) when does the location of the decoupling capacitor matter on a PCB and when it does, (b) where should the capacitor be located for effective decoupling.

V. REFERENCES

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Biographies

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Wireless Phone Threat Assessment for Aircraft Communication and Navigation Radios

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Abstract—Emissions in aircraft communication and navigation bands are measured for the latest generation of wireless phones. The two wireless technologies considered, GSM/GPRS and CDMA2000, are the latest available to general consumers in the U.S. A base-station simulator is used to control the phones. The measurements are conducted using reverberation chambers, and the results are compared against FCC and aircraft installed equipment emission limits. The results are also compared against baseline emissions from laptop computers and personal digital assistant devices that are currently allowed to operate on aircraft.

Keywords: Aircraft; interference; wireless phone; CDMA2000, GSM; GPRS; reverberation chamber

I. INTRODUCTION

Wireless markets and technologies have experienced phenomenal growth in the recent years. Two technologies that saw the most growth are wireless phones and wireless local area networks (WLANs). These technologies enabled a revolution in accessibility and productivity as they enabled consumers to have convenient access to the internet, email, instant messaging and numerous other applications.

For various reasons, use of wireless phones is currently prohibited while the aircraft is in the air. However, with a high percentage of travelers owning wireless phones, occasional unintended use, as well as unauthorized intended use is expected.

Recent flight demonstrations show that wireless phone use on airplanes is technically possible. In these demonstrations, wireless phones communicated with the on-board picocell base-stations rather than directly with the ground towers, thereby reducing the possibility of interfering with the ground cellular networks. Plane to ground communications were provided through satellite links.

Unlike aircraft installed equipment, passenger carry-on devices such as wireless phones are not required to pass the rigorous aircraft radiated field emission limits. It is therefore the goal of this study to measure the emissions from wireless phones in aviation bands and to assess interference risks to aircraft systems.

Built upon the process and results from the previous efforts [1][2], this study revisits the phone emissions topic. The current effort focuses on the latest generation of phones that are more data-capable. In specific, the two latest and popular technologies used in the US are the CDMA2000 1xRTT (1x Radio Transmission Technology) and the GSM/GPRS (General Packet Radio Service). Phones operating in 850 MHz and 1900 MHz range are addressed. Testing in both voice and data modes are conducted.

For simplicity, the terms CDMA and GSM in this paper refer to the wireless technologies unless otherwise noted. The CDMA is expanded to CDMA2000 1xRTT technology or devices. Likewise, the GSM term is expanded to GSM/GPRS technology and devices. The distinction is only made when GSM refers to voice communication mode, while GPRS refers to data mode.

II. SCOPE

Assessment of aircraft radio receiver interference is typically accomplished by addressing the three elements of the equation:

where "*A*" is the maximum RF emission from the offending device in dBm; "*B*" is the aircraft receiver maximum interference coupling factor in dB; "*-B*", in dB, is commonly referred to as the minimum interference path loss (IPL); "*C*" is the receiver's minimum in-band on-channel interference threshold in dBm.

If the minimum interference threshold, "*C*", is lower than the maximum interference signal level at the receiver's antenna port, "()", there is a potential for interference.

The emphasis of this paper is to document the measurements and results of the maximum RF emission, "*A*", from wireless phones. "*B*" and "*C*" are determined from earlier efforts [1][2] and are not addressed here due to the page limitation. However, the remaining analysis can be found in [3].
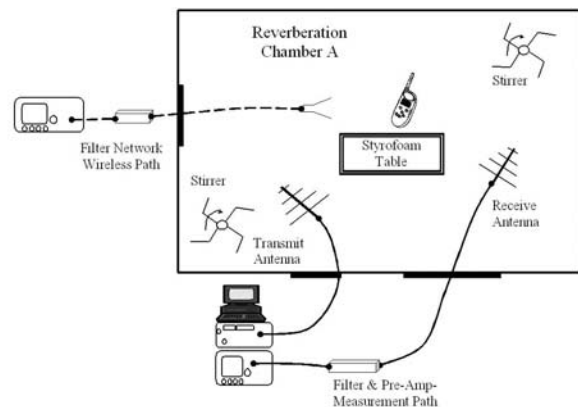

Figure 1. Reverberation chamber and wireless phone emission test configuration

Figure 2. The GSM Test Phones (not to scale)

Figure 3. The CDMA Test Phones (not to scale)

In addition, the results are restricted to unintentional emissions in and near aircraft radio spectrum. Intentional emissions, or desired emissions for the purpose of voice and data communication, are typically known or easily determined and are not considered in this study.

III. APPROACH

Various aircraft radio bands of interest were grouped into five *measurement bands* to reduce the number of measurements and test time. Aircraft radio bands that overlapped, or were near one another were grouped together, and emissions were measured across the entire combined band simultaneously. Five measurement band groups, designated as Band 1 to Band 5, covered aircraft radio bands such as Localizer (LOC), Very High Frequency Voice Communication (VHF-Com), VHF Omnidirectional Range (VOR), Glide-slope (GS), Traffic Collision Avoidance System (TCAS), Air Traffic Control Radar Beacon System (ATCRBS), Distance Measuring Equipment (DME), Global Positioning System (GPS), and Microwave Landing System (MLS). Table I correlates the measurement bands and the listed aircraft radio bands.

It is implied that high emissions anywhere in a measurement band potentially affect all systems grouped in that band. No effort is made to distinguish whether the emissions were on any specific radio band or channel.

Two reverberation chambers were used to conduct the measurements, producing results in the form of total radiated power (TRP) [4]. This method differs from the approach used in RTCA/DO-199 [5], where the equivalent power was estimated from the electric field measured at a given distance from a device-under-test. Additional details on the reverberation method testing are in the next section.

Each wireless phone was tested individually, and was controlled using a wireless base-station simulator (BSS). Located outside the test chamber, the BSS communicated with a test phone in the test chamber via a filter network and a wideband antenna. The BSS commanded the test phone to operate in various voice/data modes, frequency channels and data rates while emission data were being collected. The filter network passed the desired wireless signal while preventing any spurious emissions from the BSS from contaminating the environment in the test chamber. Fig. 1 shows the test chamber and the equipment set-up.
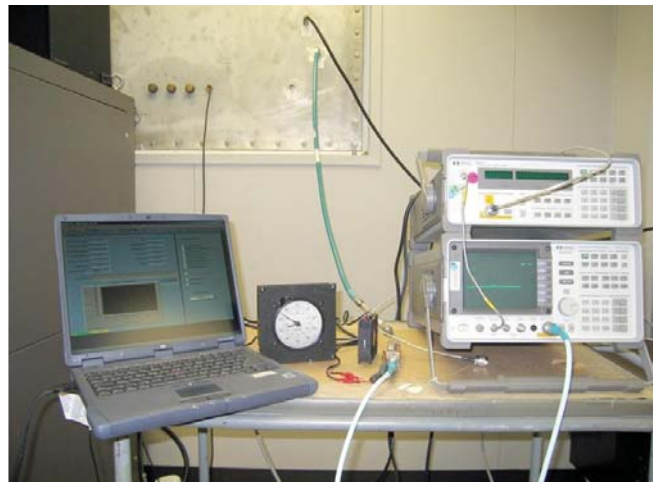

Figure 4. A sample set up in a small test chamber. The front antenna was for communicating with the phone under test.

Figure 5. Control and Data Acquisition Set-Up outside the Test Chamber.

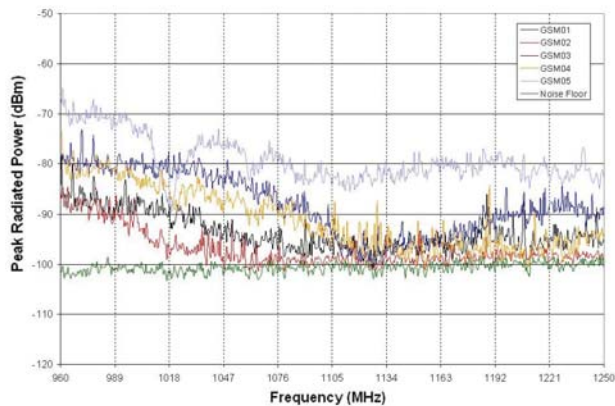*Figure 6: Sample GSM Phones Maximum Emissions in Band 3*

Figure 7. Sample CDMA Phones Maximum Emissions in Band 3

The devices considered included 17 phones using GSM technology and 16 phones using CDMA technology (Fig. 2 and 3). Most of these devices were new, and active service subscriptions were not required for communicating with a BSS. The specific brands and models can be found in [3].

The measured results were compared against the emissions from common computer laptops and PDAs previously reported in [2]. The PDAs/laptop computers emission data establish a baseline for devices that are currently allowed on an aircraft. The results were also compared against corresponding FCC wireless phone spurious emission limits, FCC Part 15 limits for non-intentional transmitters, and the RTCA aircraft installed equipment limits.

IV. WIRELESS PHONE TEST MODES

It is not the intention of this paper to compare the CDMA phones against the GSM phones. However, due to the different design features and the test modes selected, the testing and the results were grouped into two distinct groups. All the GSM phones were tested using a similar set of test modes, whereas the CDMA phones were tested using a different set of test modes. However, the test mode selections shared these common guidelines:
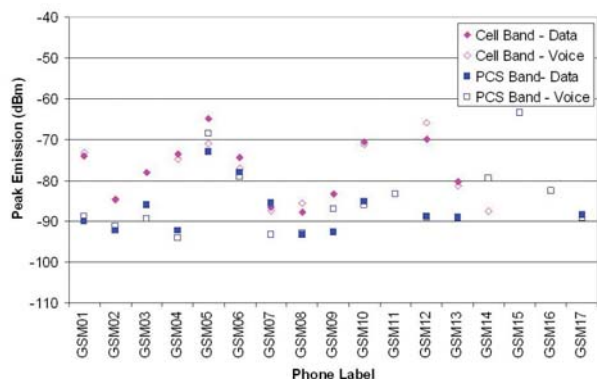
- Voice mode
- Data modes, at four different data rates

- Cellular and PCS bands (if supported by the phone)
- Five frequency channels, equally spaced, spanning across each of the cellular and PCS bands
- Maximum phone transmission power
- Idle mode and "No BSS Signal" idle mode

The actual test modes selected were dictated by the common set of capabilities of the phones and of the BSS, and typical usage. The number of test modes was also constrained by the total test time. The combinations totaled to approximately 1785 and 1680 separate measurements for the 17 GSM phones and 16 CDMA phones, respectively. Tables II and III summarize the test modes selected.

V. MEASUREMENT METHOD

A. Reverberation Chamber Test Method

Reverberation chambers were used because of their excellent repeatability, field uniformity, aspect independence, and speed. The results are in the form of total radiated power rather than in field strength. A disadvantage of testing wireless devices in reverberation chambers include occasional difficulties in establishing and maintaining connectivity with the wireless devices due to severe multipath interference.

Two reverberation chambers were used for the five measurement bands. The larger chamber, designated as Chamber A, had the lowest usable frequency of approximately 80 MHz and was
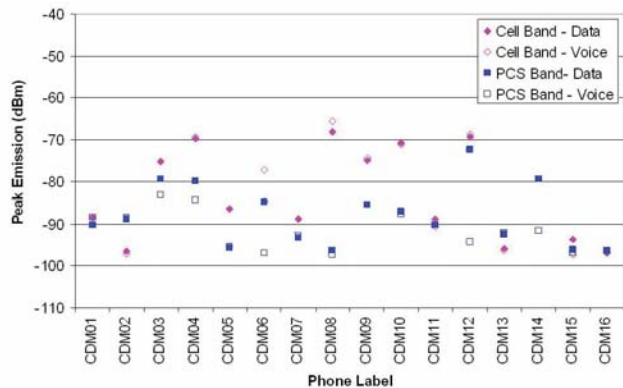

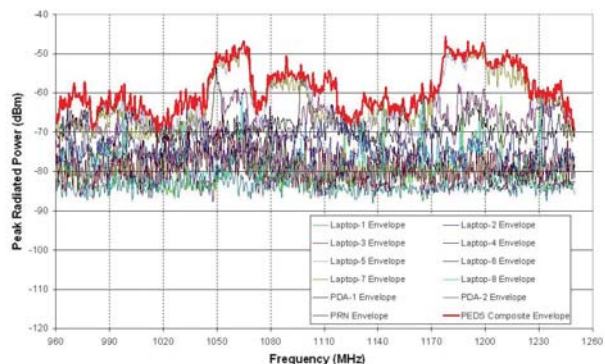*Figure 8. GM/GPRS Phones Maximum Emissions in Band 3*

Figure 9. CDMA2000 Phones Maximum Emissions in Band 3

Figure 10. Laptops/PDA Emissions in Band 3

Figure 11. Emissions from Wireless Phones and Comparison with Emission Limits

used for Band 1 and Band 2. The smaller chamber, designated as Chamber C, had the lowest usable frequency of about 350 MHz and was used for Band 3, Band 4 and Band 5. The smaller chamber has lower chamber loss, resulting in better measurement sensitivity at higher bands.

Due to the chamber quality factor and the associated chamber time constant (0.6 μsec near 100 MHz), it was assumed that most measured signals were continuous-wave (CW) or pulse modulated with 1.5 μsec pulse-width or longer [4].

The *mode-stirred* method was adopted due to ease of implementation and speed. In the mode-stirred method, the stirrer continuously rotated rather than stepped as in the *mode-tuned* method. The stirrers located in the corners of the chamber rotated at 5 rpm during both chamber calibrations and testing.

Fig. 4 and Fig. 5 show the emission test setup in a reverberation chamber, and the data acquisition system outside the test chamber. The wireless BSS was located outside the chamber to avoid contaminating the test environment.

A chamber calibration was first performed. In this step, a known level of power was delivered from the source into the chamber through the transmit antenna. The spectrum analyzer was used to record the maximum power coupled into the receive antenna (and the receive path) while performing synchronized frequency sweeps with the tracking source. The difference, in dB, between the injected power and the measured power determined the chamber calibration factor (after correcting for appropriate cable and other system losses).
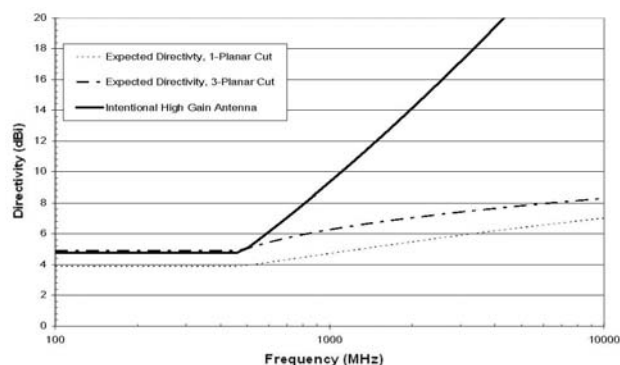
During the emission measurements, the DUT was set to operate in desired operating modes. The spectrum analyzer's trace was set on maximum hold mode while continuously sweeping over the measurement frequency band. Finally, chamber calibration factors were applied to arrive at the final total radiated power.

B. Filters and Amplifiers

Proper filtering was required for accurate measurement of spurious emissions from the wireless phones. Two separate sets of custom filters were used, one in the wireless path and the other in the measurement path. In the wireless path, the filters were to block any undesired signal from the wireless BSS from contaminating the test chamber while passing the wireless signals. In the measurement path, another set of filters were to block the high power wireless signals from overloading the measurement instruments or the pre-amplifiers while passing the desired measurement band(s). The pre-amplifiers were used in the measurement path to improve system sensitivity.

The filter network in the wireless path was positioned between the BSS and its antenna. The filter network consisted of two separate cellular and PCS band filters in parallel to pass both bands simultaneously. This set-up allows the BSS to switch seamlessly between the wireless bands without changing filters as it is necessary to test dual band phones. This set-up can also

Figure 12. Expected Directivity for a 20 cm (8 inches) Unintentional Transmitter

Table I. Emission Measurement Band Designations

Meas. Bands	Meas. Freq. Range (MHz)	Aircraft Systems Covered	Spectrum (MHz)
Band 1	105 – 140	LOC	108.1 – 111.95
		VOR	108 – 117.95
		VHF-Com	118 - 138
Band 2	325 – 340	GS	328.6 – 335.4
Band 3	960 – 1250	TCAS	1090
		ATCRBS	1030
		DME	962 - 1213
		GPS L2	1227.60
		GPS L5	1176.45
Band 4	1565 – 1585	GPS L1	1575.42 ± 2
Band 5	5020 - 5100	MLS	5031 – 5090.7

Table II. CDMA2000 Phone Test Modes

Test Modes	No. of Cell Band Channels	No. of PCS Band Channels	Test Time (minutes)
Voice	5	5	2 per channel
Data (Fundamental Chanel)	5	5	2 per channel
Data (SupplementalChannel) 9.6 kbps 38.4 kbps 153.6 kbps	 5 5 5	 5 5 5	 5 per 5 channels 5 per 5 channels 5 per 5 channels
Idle	1	1	2 per channel
Idle (No BSS Signal)	None	None	2

Table III. GSM/GPRS Phone Test Modes

Test Modes	GPRS MS Config [Down, Up]	No. of Cell Band Channels	No. of PCS Band Channels	Test Time (minutes)
Voice		5	5	2 per channel
Data (GPRS Mode)	[1,1] [2,1] [4,1] [2,2]	5 5 5 5	5 5 5 5	5 per 5 channels 5 per 5 channels 5 per 5 channels 5 per 5 channels
Idle		1	1	2 per channel
Idle (No BSS)		None	None	2

be expanded to include other frequency bands.

The filters and amplifiers were present during both the calibration and measurement. Their effects on the measurement data were automatically accounted for in the process.

VI. MEASUREMENT RESULTS

The phone test modes include combinations of voice mode, various data rates, frequency channels, and operating bands (cellular or PCS). In this paper, only the maximum emission envelopes in Band 3 are shown for a limited number of phones. The remaining data can be found in [3].

The results are grouped into CDMA and GSM groups. Sample results are shown in Fig. 6 and 7 for five phones in each group. In addition, a noise floor is shown to represent the spectrum analyzer noise floor that was processed in the same way as the data. This noise floor establishes the sensitivity of the measurement system.

Fig. 8 and 9 present the summary plots of the peak emission values for all the phones operating in combinations of voice/data modes and cellular/PCS bands. These summary charts can be used to quickly compare results and to identify phones that behave abnormally from their peers in terms of the maximum emission levels.

VII. RESULTS COMPARISON WITH ALLOWED DEVICES EMISSIONS AND REGULATORY LIMITS

A. Baseline Emissions from Laptop Computers and PDAs
Spurious radiated emissions were recorded for eight laptop computers, with each operating in five modes: idle, screensaver, file transferring, CD playing, and DVD playing. Two Personal Digital Assistants (PDA) operating in idle and file transfer modes were also considered. The maximum emission envelopes for the devices are compared against wireless phones' emissions. Again, only the results for Band 3 are shown (Fig. 10) due to page limitation. However, detailed measurement results can be found in [2].

B. FCC and Aircraft Installed Equipment Emission Limit
RTCA/DO-160 [4] Section 21 Category M emission limit is selected for comparisons with emissions from passenger carry-on devices. This limit is designated for installed equipment in the passenger cabin or in the cockpit of a transport aircraft, where apertures (such as windows) are electromagnetically significant. Similarly, FCC Part 15.109 [6] limits for unintentional radiators (such as laptop computers), and the spurious emission limits for wireless phones in the cellular [7] and PCS bands [8] are also used in the comparison.

The emission limits are converted from field strength to *effective-isotropic-radiated-power (EIRP)* using:

where E = Electric Field Intensity at distance R (V/m)
R = Distance (m).

EIRP can be converted to dBm using the 10 * log(1000*$EIRP$). Ref. [2] provides additional details on the limits and the equivalent power levels.

Table IV and Fig. 11 summarize the maximum emission levels from all the phones and compare them against the maximum laptop emissions and the emission limits. The limit value for each measurement band is conservatively chosen to be the lowest limit value of the aircraft bands within it. The results are shown in "total radiated power" (*TRP*) where as the emission limits are usually given in *EIRP* or effective-radiated-power (*ERP*). The next subsection provides an estimate of the uncertainty in the comparison due to unknown device directivity.

C. Device Directivity
Emissions measured using a reverberation chamber provide results in *TRP* within the measurement resolution bandwidth. *TRP* is different from *EIRP* and *ERP* except for antennas or devices with an isotropic radiation pattern. Rather,

where is the directivity, or maximum directive gain of the test device. Comparing *TRP* directly with *EIRP* can lead to an uncertainty equal to the . is usually difficult to measure since maximum radiation angles and mechanisms for *spurious* emissions are often not known. However, [9] provided a statistical approach to estimate the expected for unintentional emissions. Using the equations provided in [9], Fig. 12 shows the expected for the largest test wireless

Table IV. Maximum Emission from Wireless Phones in
Aircraft Bands (in dBm)

Meas. Band	Cell Band Phones (GSM & CDMA)	PCS Band Phones (GSM & CDMA)	Baseline Laptops PDAs	Aircraft Bands
Band 1	-75.3	-76.8	-63.3	LOC, VOR, VHF-Com
Band 2	-79.5	-75.8	-58.7	GS
Band 3	-64.7	-63.3	-45.7	TCAS, DME, GPS L2
Band 4	-85.8	-66.5	-55.8	GPS L1
Band 5	-43.8	-63.8	-77.0	MLS

phone (20 cm maximum dimension), which varies between 5 and 8 dB for the five measurement bands.

VIII. SUMMARY AND CONCLUSIONS

The following summary and conclusions were made based on the presented data as well as the more detailed results reported in [3]:

- The 33 wireless phones tested did not generate higher emissions than standard laptop computers in most aircraft bands considered (Bands 1-4). The exception is the MLS band (Band 5), where the emissions from the phone exceeded the emissions from the laptop computers.
- The spurious emissions from the phones were also below the aircraft installed equipment limits (RTCA/DO-160 Cat. M), even with the consideration of the 5 to 8 dB uncertainty associated with the phones expected directivity.
- Voice and data mode spurious emissions were generally similar (within 2-5 dB) in most cases. In addition, emission results for cellular band versus PCS band operations were similar for measurement in Band 1 and Band 2. It was not the case for the remaining Band 3 to Band 5.

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Biographies

Truong Nguyen received his B.S.E.E. and M.S.E.E. both from The Ohio State University, Columbus, OH, in 1987 and 1990, respectively. He was with Research Triangle Institute, Hampton, VA from 1990 to 1994, where he conducted research on computation methods, compact range radar-cross-section (RCS) and antenna measurements for aerospace applications. He joined NASA Langley Research Center, Hampton, VA in 1994. Since then, he has conducted research on reverberation chamber test methods for aircraft RF immunity and emission measurements applications. His current interests include consumer electronics aircraft compatibility, high intensity radiated fields (HIRF) and emission measurement techniques, numerical methods, RCS and antennas.

Truong Nguyen served on the RTCA/SC-135 committee to develop DO-160 Revision 1, Section 20 aircraft HIRF reverberation test procedure. From 1998-1999, he assisted the National Transportation Safety Board in the TWA-800 accident investigation regarding RF field effects. He co-authored several reports on RF emissions from intentionally transmitting portable electronic devices (PEDs) and compatibilities with aircraft radio receivers. He is currently serving on the RTCA/SC-202 committee to develop allowance process and guidance on aircraft use of transmitting PEDs.

Sandra Koppen received a Bachelor of Science Degree in Computer Science from Old Dominion University in 1987. She has worked in the NASA Langley Research Center High Intensity Radiated Fields (HIRF) Laboratory for thirteen years as a computer analyst with Lockheed Martin Corp. and as electronics engineer with NASA. Her interests include evaluation of electromagnetic field effects on avionic systems for aerospace applications, reverberation chamber characterizations and operations. She has performed research on the assessment of wireless phone and portable electronic device (PED) interference threats to aircraft communication and navigation systems. She has served on the RTCA/SC-202 committee which is developing guidelines for assessing the risk of interference due to the use of transmitting PEDs on aircraft. She has co-authored reports on the effects of RF emissions from PEDs on aircraft receivers.

Laura Smith received her Bachelor of Science in Mathematics, with a minor in Physics, from Christopher Newport University in Newport News, VA in 1993. She received her Master of Arts in Mathematics from the College of William and Mary in Williamsburg, VA in 2001. Ms. Smith has been employed with NASA Langley Research Center since 1983. She is currently a Computer Engineer in the Safety-Critical Avionics Systems Branch. Her research interests include EMI measurement techniques, mathematical modeling techniques, and statistical analysis. She has also performed assessments of electromagnetic interference threats to aircraft systems.

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TEM Cells for Whole Aircraft EMV Testing

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Abstract—*Transverse Electromagnetic (TEM) cells offer one solution to the problem of EMV testing of whole vehicles at lower frequencies. This paper discusses computational electromagnetics (CEM) modelling used to investigate various TEM cell configurations in order to optimize the method for testing a military aircraft. A baseline for the study was achieved by comparing a simulated aircraft in the DSTO TEM cell, on an Open Area Test Site (OATS) and in free space. The model was then used to investigate improvements to the TEM cell performance by modifying its design. It is shown that by changing from a solid to wire septum, gains are achieved in the low frequency performance of the cell. We also report on studies of active TE mode resonance cancellation. All results are discussed with respect to implications for future TEM cell designs.*

I. Introduction

Today's technology-laden military aircraft are exposed to a myriad of RF (Radio Frequency) emissions while undertaking their defined operational roles. Electromagnetic Vulnerability (EMV) testing is therefore an important part of ensuring air platform reliability. A reverberation chamber (RC) was built and tested at the Defence Science and Technology Organisation (DSTO) in South Australia for EMV testing and works well at frequencies 30 MHz where mode density is sufficiently high.

Unfortunately the RC does not access the HF region (2 - 30 MHz) of the communication spectrum. In order to conduct EMV testing in this HF frequency range, DSTO currently uses an open area test site (OATS) together with the bulk current injection (BCI) technique. However, this method is limited by restrictions on spectrum use, inaccuracies inherent in BCI and equipment maintainability due to weather exposure. Our current research program is looking at an alternate EMV testing method in the HF range using a TEM cell. In the literature, TEM cells have been proposed for whole vehicle testing either as a separate test facility [1], [2], or in a hybrid configuration with an RC [3]–[5]. We are considering both of these aspects in our study, but initially focusing on the TEM cell only.

The TEM cell design, otherwise know as the "Crawford style" [6], is not without its limitations. Confined test volume, frequency limits due to the appearance of higher order modes, and polarization restrictions are problems which have been the main motivation behind many of the TEM cell studies. Other methods of constructing TEM cells have been proposed and modeled in which improved performance has been obtained through changes in septum design and loading methods. For example, Carbonini [7] reports on a cell with double polarization and balanced wire septa, the X-TEM cell, resulting in optimization of the test volume dimensions.

An asymmetric "Crawford style" TEM cell exists at DSTO for research purposes. It was intended to be a scale model of what could be implemented in the existing RC to form a hybrid system, and its proportions are so based. The outer dimensions transverse to the propagation direction are 2.335 m by 1.27 m, and length of the parallel section is 2.26 m. The tapered sections are 1.114 m long and the feed points of the solid metal septum are offset 0.29 m from the cell wall.

The major aim of our study is to investigate the potential for EMV testing a whole aircraft using a TEM cell. We intend to investigate various TEM cell designs initially through Computational Electromagnetic (CEM) modelling and then progress on to the measurement of a physical system once a promising design has been identified. This paper details our initial experiments conducted on a CEM model of the DSTO TEM cell [8] using a Method of Moments (MoM) approach. The first section describes our work on establishing a baseline for our CEM model by validating it with measurements carried out on the physical cell. This was developed further by extending the model to include a test subject aircraft, with its performance being compared to the free space and OATS environments. The last section of the paper describes the work conducted to improve the performance of the DSTO TEM cell. This includes modifying the septum design to increase the uniform field test region. In addition, we will report on active mode cancellation work aimed at controlling the first TE cavity mode.
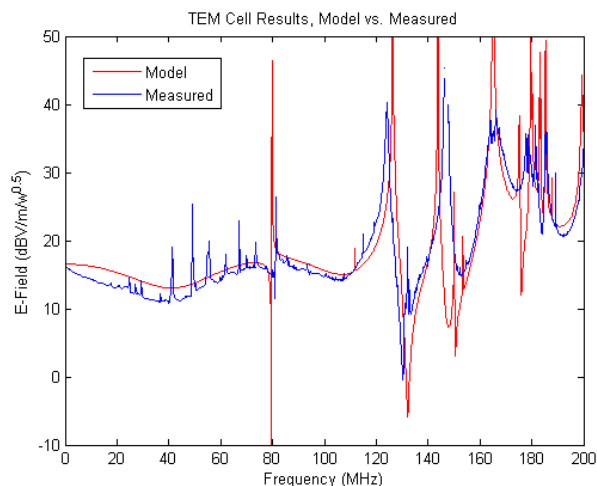
Fig.1. Comparison between measured and numerical results for the DSTO TEM cell.

II. Model Validation

The empty DSTO TEM cell was modeled using a MoM approach in order to calculate the near electric field strengths for a series of 9 points in the cell's test region. Measurements were conducted at equivalent points inside the physical TEM cell, and used to validate the MoM model. The comparison of the two data sets for a central point in the test region is shown in Figure 1.

The results show the desired TEM mode is present below 79.8 MHz and between the peaks at 79.8 MHz and 123 MHz. It is seen that the measurements and model agree very well upon the level of field for the TEM mode with a discrepancy of less than 2 dB. Above the 123 MHz peak, it is not apparent what the relative contributions are from TEM and resonant modes. Total field levels agree well, however. It is clear that all the resonances in the model are present in the measurements with some disagreement in frequency by approximately 2.5 MHz.

Some resonant peaks are seen in the measurements below 79.8 MHz, which disagrees with the theoretical minimum frequency for resonance in a cavity of this size and with the numerical model. These peaks are due to the use of the broadband E field probe together with third harmonic distortion in the amplifier.

Considering the results for all nine observation points we find that the DSTO Cell conforms to the accepted 1/3 volume uniform test region [6].

III. TEM Cell Performance Metrics

Henceforth, the TEM cell model dimensions have been scaled up by a factor of 4.7 to represent the intended size of the cell for whole aircraft testing. Therefore, the TEresonance at 79.8 MHz mentioned above occurs at 79.76/4.7 = 16.97 MHz in the scaled-up cell.

A. Models

The Aermacchi MB326 (Macchi) aircraft was acquired in 1967 for use with the Royal Australian Air Force (RAAF) and Royal Australian Navy (RAN), where it served as mainly a trainer aircraft. Now out of service, a Macchi aircraft has been obtained
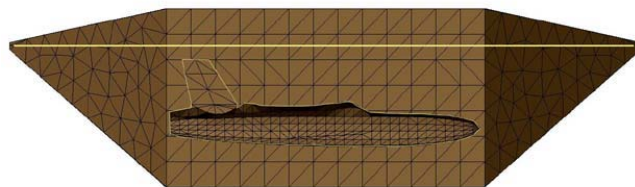

Fig. 2. MoM model of the Macchi aircraft in the DSTO TEM cell.

by DSTO for its EMV research program. Inside the validated TEM cell model, we added a numerical model Macchi jet aircraft, as a test object. In addition, we have placed a numerical model of a Macchi on the DSTO open area test site (OATS) to assess the LLSC(low level swept coupling)-BCI low frequency testing technique. The CEM model of the Macchi in the TEM cell is shown in Figure 2.

The Macchi model was meshed in an engineering modelling tool, FEMAP, from a CAD file and then entered into FEKO. FEKO [9] is a commercial electromagnetic software package capable of hybrid UTD/MoM operation. We used the MoM capability, which is based on the well known Rao-Wilton-Glisson basis functions. The TEM cell and OATS ground plane are both constructed in FEKO from triangular surface elements. The free-space and OATS environments used a standard FEKO plane wave source allowing multiple source directions and polarisations. For the TEM cell, narrow triangular plates were used to connect each septum end to its adjacent outer shell region. This construction mimics the coaxial connectors at the ends, the shields of which are connected to the outer chamber, and the inners of which are connected to the septum tips. One wire was then driven with a voltage source, and the other was loaded with a 50 resistance.

In order to compare the three Macchi model configurations, we needed to calibrate the TEM cell and OATS to the free space case. In free space we set the plane wave source to 1 V/m. The driving voltage required in the TEM cell was calculated by finding the average field strength for a volume inside the empty cell at 10 MHz. Using this average field, the driving voltage was scaled up to produce an average field strength of 1 V/m. This voltage was found to be 4.6 V. For the OATS, the only case which has to be calculated is where the plane wave source is horizontally polarised. This is due to the boundary conditions imposed by the horizontal ground plane. The electric field was calculated 2 m above the centre of the ground plane for all the frequencies. These values were used as scaling factors at the various frequencies for the results obtained when the Macchi was present. This reflects normal OATS calibration practice in the field.

B. Near Field Metric

TEM cell design calls generally for minimum size due to the need to keep resonance frequencies high, and to reduce required input power levels. Additionally, in DSTO's case, a desire exists to modify the existing RC. Thus DSTO is pushing the limits of useable TEM cell volume, as a typical jet fighter occupies a considerably greater fraction of the TEM cell volume than is generally felt to be ideal. The concern arises: What could the effects be of the proximity of the aircraft appendages to the TEM cell walls? An obvious possibility is
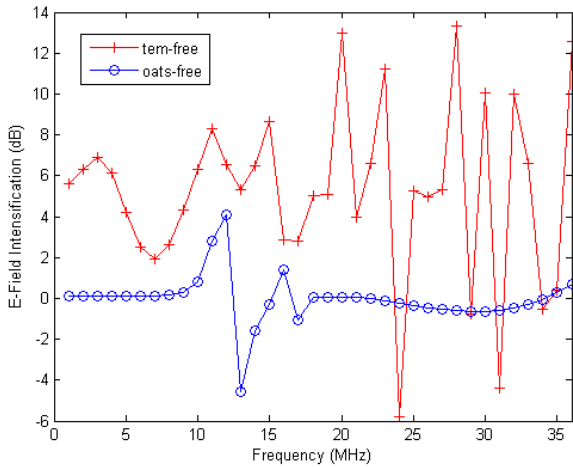
Fig. 3. Electric field intensification for the vertical stabilizer observation point.

the intensification of electric field strengths in these areas, as charge accumulation on aircraft appendages leads to induction of corresponding charges on the TEM cell surfaces and vice versa. Note that it is of no use to compare the fields around the aircraft to 1V/m, as we are considering the total field, not the incident field. Even in free space intensification of field strengths will occur near terminal points of the airframe. Near electric field strength is the determining factor in coupling to projecting conductors including monopole antennas, hence it is important the test method produces realistic levels. To this end we have investigated the electric field intensification around the Macchi aircraft for the TEM Cell, OATS and free space cases.

Field observation points were chosen at a distance of 20 cm from key physical features on the Macchi aircraft including wing, nose and vertical stabilizer. For frequencies from 1 MHz to 36 MHz at 1 MHz increments, the electric field strengths at these locations were calculated for each of the three models: TEM cell; OATS; and free space. To maximise spacing from the cell walls, the Macchi aircraft nose-to-tail axis was rotated 45 relative to the source-load axis of the TEM cell. For the Macchi in free space and on the OATS, a vertically polarised plane wave source was used to simulate the feed conditions in the TEM cell. The results for the vertical stabilizer are shown in Figure 3, where the curves represent the TEM cell and OATS electric field strengths relative to free space in dB. A similar plot was also generated for the other 8 observation points. We show only the vertical stabilizer here as an example.

Indication of the ability of a particular method to reproduce the field conditions seen by the Macchi aircraft in free space is given by the curve's closeness to the 0 dB line. With this in mind, we see that for the vertical stabilizer position, the OATS method is better than the DSTO TEM cell. It shows near perfect reproduction of the expected field levels except at 12 MHz and 13 MHz where we see an airframe resonance due to the aircraft being above a ground plane. The TEM cell, however, shows an intensification in the field, varying between 2 and 8 dB for frequencies between 1 MHz and 20 MHz. This is not surprising since the tip of the vertical stabilizer is in close proximity to the TEM cell septum (see Figure 2). For frequencies above 20 MHz we see large fluctuations in the field levels due to TEM cell cavity resonances.

In this data, the TEM resonance may have been missed by the data point frequency step of 1 MHz.

C. Surface Current Metric

As well as external field levels around the aircraft, surface currents are an important component of EMV testing. It is the surface currents on the aircraft skin which induce currents on the cables running through the airframe. These currents are of interest since they can cause unpredictable behaviour within the avionics systems. To this end we have compared the performance of the two testing methods using a surface current analysis.

The aim was to compare the surface currents on the Macchi aircraft between the three configurations: free space; OATS; and TEM cell. The MoM method of calculation provides the surface current for each triangle within the surface mesh of the computational model. To minimise the volume of data used for the comparison, a select number of surface mesh triangles were chosen as current observation sites. Sites were chosen to relate to the field observation points described in the last section. One site was chosen on each wing, nose, cockpit, horizontal and vertical stabilizers.

Surface currents were calculated using FEKO for frequencies between 1 MHz and 36 MHz at 1 MHz intervals. To obtain a more representative baseline for comparison, a range of source directions and polarisations relative to the Macchi aircraft were used for the OATS and free space calculations (in essence this reproduces the low-level swept-coupling (LLSC) calibration techniques used for OATS testing). The resultant series of OATS and free space curves for each direction and polarisation combination, were combined by taking the maximum current at each frequency. This produced one curve for the OATS and one for free space. The TEM cell and OATS surface current results were divided by the free space currents, again providing a relative comparison. The vertical stabilizer results are shown in Figure 4 as an example. Again the ability of the test method to reproduce the surface currents seen on the Macchi aircraft in free space is gauged by the data's proximity to the 0 dB line in the plot. Note that the plot contains two sets of TEM cell results, one with the Macchi parallel with the direction of wave travel and the other with the Macchi at 45 to the direction of travel. This was done to gauge the effect of orientation in the TEM cell.

In Figure 4 we see that for frequencies above 15 MHz the OATS results are closer to the 0 dB line than the TEM cell. However, for frequencies below 15 MHz the TEM cell performs slightly better, with the OATS results suffering from a large current intensification, of 20 dB, at 6-7 MHz. On comparing the two TEM cell results we see there is little effect on the results after changing the orientation of the Macchi aircraft. In considering the results obtained for all seven observation triangles it is clear that the OATS performs better than the DSTO TEM cell. Particularly for frequencies above 15 MHz where the TEM cell suffers from the onset of cavity resonances. However, since the DSTO TEM cell is not yet optimized for aircraft testing, the results suggest many areas for future investigation.

IV. Novel TEM Cell Design

A. Septum Modification

In section II, our CEM modelling technique for TEM cells was validated. In section III a performance baseline was established for
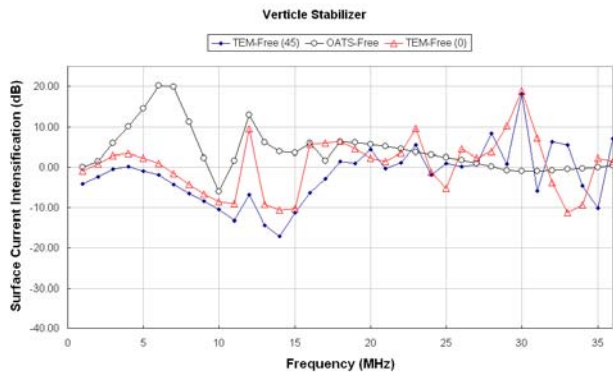
Fig. 4. Surface current intensification for the vertical stabilizer observation triangle on the Macchi skin.
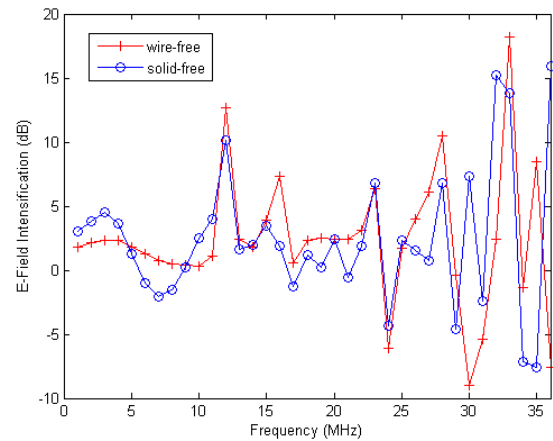

Fig. 5. Electric field intensification for the vertical stabilizer observation point. Comparison between DSTO TEM cell with a solid septum and with a wire array septum.

the DSTO TEM cell by looking at electric field and surface current intensification. We now use these performance measures to improve on the DSTO TEM cell by investigating novel TEM cell designs.

Carbonini {10} studied a TEM cell with a wire array septum instead of a metal sheet, known as a WTEM cell. He reported gains in useable test volume in addition to decreased capacitive coupling between the DUT (Device Under Test) and cell structure. We therefore replaced the metal septum in the DSTO TEM cell with a wire array. Although Carbonini's WTEM cell adopted a GTEM type construction at one end, we have only changed the septum in our design as an initial step.

The TEM cell computational model shown in Figure 2 was again used with the solid septum replaced by a wire array. Each of the 11 wires were given a load impedance of 550 giving a combined load of 50 at one end of the septum. The Macchi's height of 2 m above the TEM cell floor used in section III-A, was reduced to 1.45 m. This produces a vertical stabilizer - septum separation greater than that between the septum wires, reducing local field distortions. The near field metric was utilized where field levels around the Macchi aircraft were calculated from 1 MHz to 36 MHz at 1 MHz intervals. The results for the vertical stabilizer are shown in Figure 5.

The electric field results show that below 10 MHz, the field intensification above the vertical stabiliser is reduced from 7dB to 2dB. By utilising a wire septum the degree of coupling between the Macchi and the septum has been reduced. There is, however, no improvement above 10 MHz where the dominant effect is cavity resonances and not DUT capacitive coupling.

B. Active Cancellation
It has already been noted, that the whole aircraft TEM cell has a TE resonance at 16.97 MHz. Such non-TEM modes, while desirable in reverberation chambers, present serious problems in the TEM cell. Destructively high field levels can easily be reached with high Q resonances. Note the increase in field levels of order 25 dB measured in Figure 1. Furthermore, the resonant mode field distribution can cancel and otherwise distort the TEM field distribution.

The approaches used in the literature and in commercial TEM cells use various forms of passive absorber material, which may either be a ferrite or carbon loaded material. To be well-coupled to the resonant modes, while not reducing the TEM mode, the absorber material needs to be appropriately distributed. It is often distributed over a terminating wall, as in the

GTEM cell. While such methods are technically proven for equipment scale use, they are not the most economical for scaling up to the size required for a whole-aircraft test TEM cell. It is clear that the volume and hence cost of the material would increase with the cube of the TEM cell scale factor. If active mode cancellation is applied, the scale factor is largely irrelevant to the complexity and hence cost of the system. The number of modes cancelled is the main determinant of complexity and this number is independent of scale factor.

Active cancellation has been applied to acoustic noise reduction, where significant improvements have been achieved in, for example, air-conditioning duct low frequency noise levels. The principle is to inject the correct phase and amplitude of signal from a loud speaker to precisely cancel the noise component. Considerable complexity comes into the design of the feedback loop gain characteristics to ensure optimal operation, especially in order to accommodate changes in the system. Clearly, deficiencies in the feedback loop design could result in oscillation and the creation of a worse problem. To the author's knowledge, active mode cancellation has not been applied to TEM cell resonances in the literature before.

For the early work presented here, a number of simplifications of the problem are accepted: The empty TEM cell is considered in order to improve the clarity of the process. Once the method has been fully developed, we plan to test the sensitivity of the technique to the introduction of aircraft. Furthermore, an active cancellation method is applied to only the first cavity resonance, TE, which occurs at 16.97 MHz (see section III). However, the next resonance occurs at 26 MHz, so this single application of the technique has almost doubled the available bandwidth. In the final simplification, the method is not demonstrated as a feedback process, but is operated in open loop, after computing the required cancellation loop drive voltage and phase.

Firstly, a suitable probe was designed which would couple well into the TE mode but very poorly to the TEM mode. Consideration of the TEM mode reveals that, like a coaxial line, the currents are primarily axial on the cell walls. Conversely, the TE mode has significant transverse currents on the side walls, which converge to zero at points on the top and bottom surfaces parallel to the septum. A loop probe centrally placed on the cell side

walls and transversely oriented will thus strongly couple to the resonant mode and very weakly to the TEM mode. A semi-circular loop was used with a central feed location to further reduce sensitivity to normal electric fields, which are present in both modes.

In the open-loop demonstration, a suitable voltage source is placed at the midpoint on the wire loop while the septum is driven normally. The loop drive voltage must be chosen in the correct complex ratio to the septum drive voltage in order to cancel the resonance.

Therefore, the constants of proportionality between the loop and septum drive voltages and the electric field strengths at the centre of the cell were found at the resonance peak frequency of 16.97 MHz for the cell driven by loop and septum alone:

and

Complete field cancellation at the test point could thus be achieved by using the value:

for the loop drive voltage. However, we wanted to retain the TEM mode component of the field, which can be seen from the Figure 6 to be 20dB smaller than the resonant mode. Therefore, the TEM mode constant, , must be extracted before the cancellation is applied otherwise it will be actively cancelled also. The electric field strength was calculated at frequency points either side of the resonance: at 15.2 MHz and 18.74 MHz, which are in regions of purely TEM operation. The average of the electric field strength for the two frequencies was used to approximate similarly to equation 1. Thus, the resonance mode constant, . The voltage on the loop required for cancellation of the resonance field component alone is finally given by:

If this is applied to the model we get a 20 dB decrease in the total field, which is now comparable in magnitude and form to the pure TEM field distributions at the adjacent frequencies, as shown in Figure 6.

The aim for future work in the area is to develop the technique to become a feedback system whereby two wire loops are placed in the TEM cell on either side of the cavity. One loop is used to measure the residual level of the TE mode, which passes through a suitable gain and phase circuit to the other loop where the canceling field is injected. The method is readily modeled in Method of Moments by adding a value to the matrix element representing the artificial propagation from the sense loop to the injection loop. The matrix then becomes asymmetric, which represents the presence of non-linear elements in the feedback path removing the property of reciprocity. The technique has been commenced and shows equivalent performance to that shown in Figure 6.
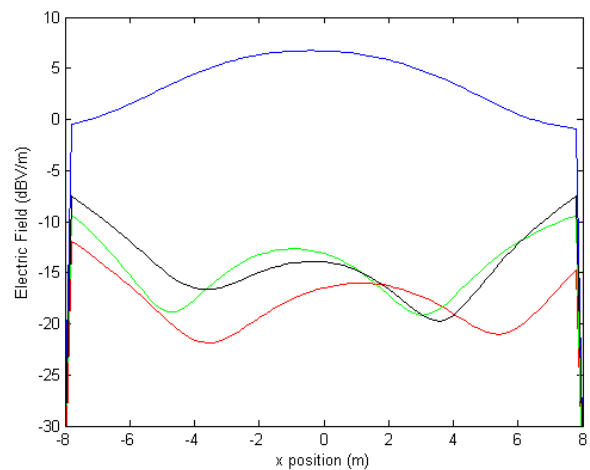

Fig. 6. *Electric Field transverse to propagation direction in the TEM cell at the midpoint between septum and cell floor for various frequencies. The Blue line at f=16.97 MHz shows the cosine-like variation of the uncancelled TE mode which swamps the TEM mode. The Black line also at f=16.97 MHz shows the effect of active cancellation. The Red line at f=15.2 MHz and the Green line at f=18.74 MHz show adjacent pure TEM mode fields.*

V. Conclusion

In this study we have validated a computational electromagnetics model of the DSTO TEM cell using measured results. In addition, we have shown the importance of using the two techniques in tandem to acquire a more accurate picture of the system. Considering the empty TEM cell results scaled up to the RC dimensions, we see TEM behaviour in the region below 17 MHz and also between 17 MHz and 26 MHz.

We have also described a metric for measuring the performance of a loaded TEM cell and OATS compared with free space, using field and surface current intensifications. The results have indicated that of the two techniques, the OATS performs closer to the free space case than the TEM cell. The TEM cell suffers from restrictions on the volume available for testing in addition to non-uniformity caused by natural resonances of the cell's cavity.

The initial investigations into the use of a wire septum have shown reduced near-field intensification where the vertical stabilizer approaches the septum. Above 17 MHz where cavity resonances dominate, the active mode cancellation technique has initially shown promise. Future work will involve investigation into feedback based active cancellation and active cancellation of higher order modes up to 30 MHz.

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